NEUROPIXELS ONEBOX

Technical User Manual

December 6, 2024

Important Information

THE NEUROPIXELS PROBES **ARE ONLY INTENDED FOR RESEARCH USE ONLY ("RUO") IN NON-HUMAN SUBJECTS** SUCH AS SMALL ANIMALS INCLUDING RODENTS AND NON-HUMAN PRIMATES. THESE NEUROPIXELS PROBES **SHOULD NOT BE USED IN HUMANS AND ARE NOT MANUFACTURED OR APPROVED FOR HUMAN USE**. THEY HAVE **NO PROVEN HUMAN EFFICACY AND ARE NOT INDICATED FOR HUMAN USE OR ANY FORM OF CLINICAL USE**.

About Neuropixels

The Neuropixels 1.0 neural probe is an advanced silicon CMOS digital integrated microsystem and a tool for neuroscience research. It was developed through a collaboration funded by Howard Hughes Medical Institute (HHMI), Wellcome Trust, Gatsby Charitable Foundation and Allen Institute for Brain Science. Probes were designed, developed and fabricated at imec, Leuven Belgium in collaboration with HHMI Janelia Research Campus, Allen Institute for Brain Science and University College London.

Legal Disclaimer

Revision history

Version	Date	Description	Responsible
V1.0.0	November 21ST ,2024	Initial customer release. Layout change. Add links to Open Ephys and SpikeGLX.	JP, RH
V1.0.1	December 6th ,2024	Update chapter references.	JP, RH

Related documents:

Table of contents

List of abbreviations

ADC	Analog-to-Digital Converter
AP	Action Potential
API	Application Programming Interface
DAC	Digital-to-Analog Converter
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read-Only Memory
FIFO	First-in, first-out
FPGA	Field Programmable Gate Array
I/O	Input/Output
LED	Light-emitting Diode
LFP	Local Field Potential
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed Circuit Board
PC	Personal Computer
PXIe	PCI Express eXtensions for Instrumentation
P/N	Part Number
SDR	Shrunk Delta Ribbon
SMA	SubMiniature version A
S/N	Serial Number
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
USB-C	Universal Serial Bus Type-C
ZIF	Zero Insertion Force

Definition of Technical Terms

- **Control system**: System components required to enable control of and data streaming from Neuropixels probes. These entail the headstage, interface cable and PXIe acquisition module or OneBox.
- **Dock:** the headstage can connect to one or two probes, depending on the probe type, using one or two ZIF connectors. Each ZIF connector is referred to as dock.
- **Driver**: The software driver API, required by the probe end users to communicate to the system and to develop custom application software.
- **Enclustra FPGA module:** FPGA plug-in module inside the OneBox.
- **Headstage**: Miniature board that enables reliable power supply to the probe and is essential for bi-directional data communication from/to the probe.
- **Interface Cable**: Thin and flexible cable for power and bidirectional data transmission between headstage and PXIe acquisition module or OneBox.
- **OneBox:** stand-alone module which acquires data from the probe and transmits to a PC over a USB3.0 interface
- **Port:** The USB-C connector on the PXIe acquisition module or on the OneBox in which the interface cable to the headstage is plugged in.
- **PXIe Acquisition module:** PXI-based acquisition module for Neuropixels probes, to transfer data from the headstage to the PC.
- **PXIe Chassis**: Houses PXIe modules and connects them with a high-performance backplane that offers timing and synchronization capabilities.
- **SDR breakout board**: PCB with BNC connectors providing easy access to the I/O signals of OneBox.
- **SerDes**: combination of serializer and deserializer chip.
- **Slot:** a slot is a position in the PXIe chassis, in which the Neuropixels PXIe Acquisition module is inserted. The OneBox module is mapped to a virtual slot number.

1 About this manual

This document describes the key features of the OneBox system and provides installation and user guidelines.

The system consists of:

- OneBox module
- Power cable and adapter
- USB 3.0 cable

This manual is valid for OneBox version 4.20, and minimum API version 3.70.2, minimum FPGA version 3.3 Build 134.

OneBox can be used with the GUIs from Open Ephys and SpikeGLX. Please consult the Quick Start Guides via these links:

- Open Ephys Quick Start Guide
- SpikeGLX Quick Start Guide

2 Installation and Configuration

2.1 Driver

Before connecting the OneBox system the first time to a PC, it is required to install the FTDI driver on the PC. The driver is provided by the manufacturer (FTDI) of the USB interface chip, which is used on the OneBox system for handling USB communication between the OneBox system and the PC.

The OneBox system uses the FT601 chip. Therefore, the correct driver to install is the D3xx driver. The driver files can be downloaded from the FTDI website: https://www.ftdichip.com/Drivers/D3XX.htm. **The minimum required FDTI driver is 1.0.3.8.**

Follow the driver installation procedure as provided by FTDI: AN_396 FTDI D3XX Driver Installation Guide.

After installation of the FTDI driver, verify whether the OneBox system is correctly recognized by the PC: Plug the power supply adapter into a wall socket and in the power supply connector of the OneBox. Switch on the OneBox. Connect the OneBox to the PC using the USB 3.0 cable. Open the Device Manager window. The Device Manager lists 'FTDI FT601 USB 3.0 Bridge Device' under 'Universal Serial Bus controllers', which indicates a successful installation.

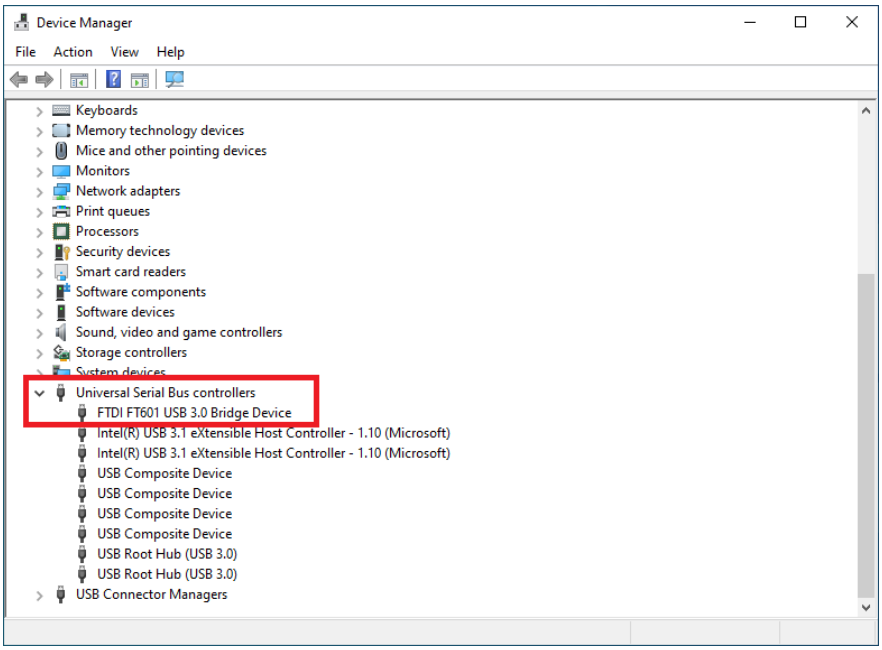

Figure 1: Device Manager after installation.

2.2 OneBox FPGA programmable logic upgrade

The OneBox system hardware is delivered preconfigured by IMEC. No further configuration is required.

The method for loading the programmable logic code to the OneBox FPGA differs from the method used in the Neuropixels PXIe Acquisition module.

The boot code memory on the OneBox contains only a basic code which enables the USB interface and communication with the API. When the API connects to the OneBox, it loads the runtime code to the OneBox FPGA. This is a very quick process which takes less than a second.

The basic boot code does not require updates, as it does not contain any code specific to the operation of the probes or the OneBox system. Therefore, it is not necessary to upgrade the boot code on the FPGA. Any required updates to the runtime code are done by a new version release of the API.

When switching between API versions while the OneBox is up and has already booted, a manual restart (power cycling) of the OneBox is required.

2.3 FTDI Configuration utility

FTDI provides a tool to read/write configuration parameters to the FT601 USB interface chip.

The FT601 USB interface chip is configured by IMEC before delivery of the OneBox system. It is therefore not required for the user to use this configuration utility. Furthermore, making changes to the configuration parameters of the USB interface chip might result in the system being no longer recognized by the Neuropixels API.

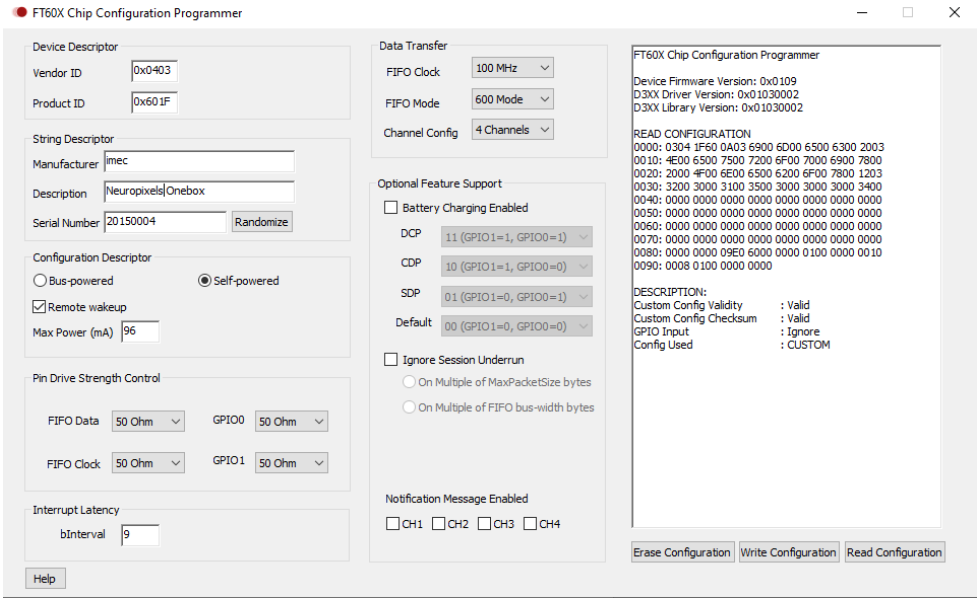

Figure 2: Screenshot of the FTDI Configuration utility, for a OneBox system.

3 OneBox hardware description

3.1 General overview

The OneBox system is intended to use Neuropixels probes without purchasing a PXIe chassis, PXIe controller, and Neuropixels PXIe acquisition module. This allows users who plan experiments with only one to four Neuropixels probes to use the probes with a limited investment. The hardware is compatible with Neuropixels 1.0 and 2.0, UHD, NHP, probes and headstages.

The system contains 2 PCBs: a motherboard which contains the deserializers, ADC, DAC, USB interface and connectors and an Enclustra ZX-5 plug-in module.

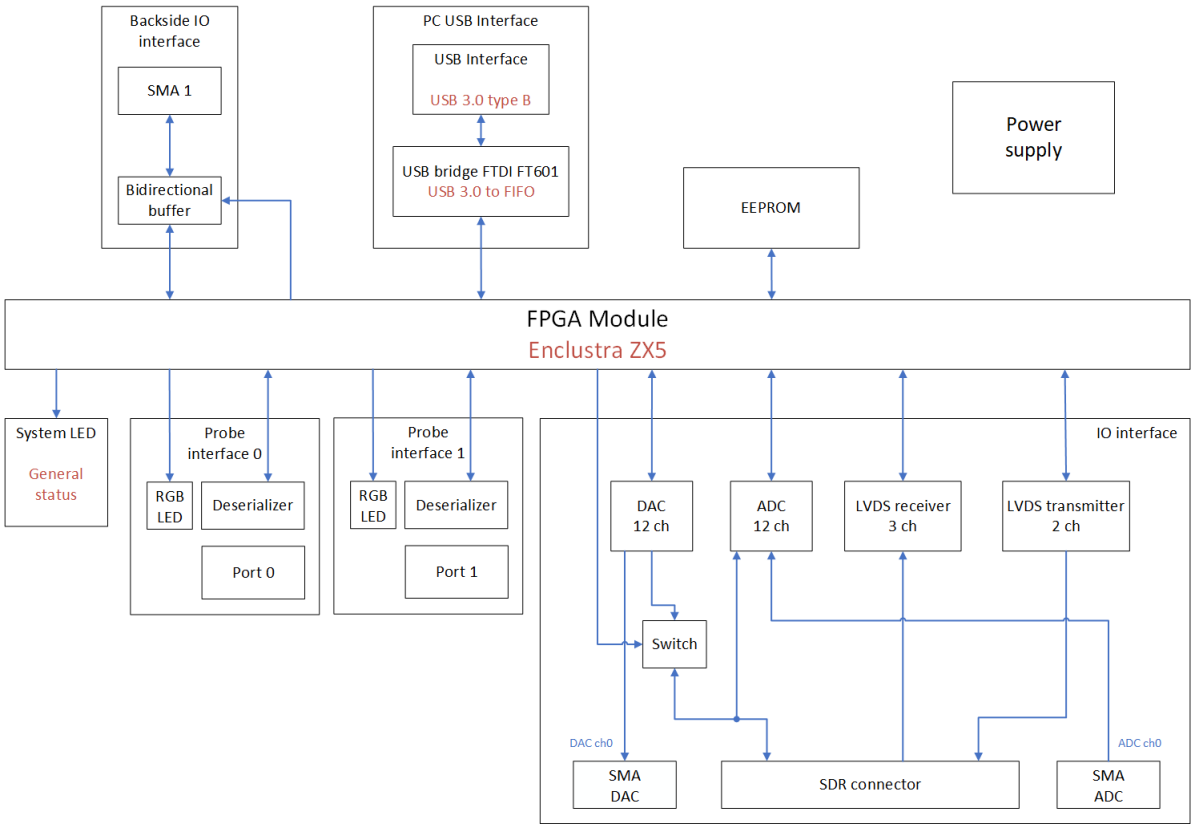

Figure 3: Block diagram of the OneBox system.

3.1.1 FPGA

The FPGA module (Enclustra ZX5: Xilinx Zynq-7 SOC, 1 GB DDR) is the core of the OneBox system. This component interfaces with the probe/headstage interface, processes, buffers and transmits data to the USB interface. The FPGA interface also communicates with the ADC, DAC and LVDS components.

The programmable logic for the FPGA is loaded in two stages: the first-stage boot loader loads the programmable logic when the FPGA is switched on. This logic enables USB communication. The warm boot code is loaded by the API to the FPGA when the API connects to the OneBox system.

3.1.2 DAC

The DAC is used to generate auxiliary output signals, both analog and digital. It is possible to output a selectable neural data channel via the DAC. The DAC is controlled by the FPGA component. The DAC and the signals which are generated by the DAC are configured with API functions.

The selected DAC is the Analog Devices AD5766, a 16-channel, 16-bit DAC. The DAC output buffers have 20 mA source/sink current capability. The DAC output voltage range is set to ±5 V.

Only the first 12 of 16 channels are available to the user. The DAC output channels are accessible via the front panel DAC SMA (channel 0), and via the SDR connector (channel 0-11).

Caution: The outputs of the DAC and the inputs of the ADC share the same pins on the SDR connector. The DAC output can be interrupted with a switch, which is controlled via the API. When connecting an external source to an ADC input channel, it is important to disconnect the corresponding DAC output channel with the switch.

3.1.3 ADC

The OneBox system features the Analog Devices ADC AD7616-P, a 16-channel, 16-bit ADC. The ADC is implemented on the OneBox system with single ended inputs. The available input voltage ranges are ±2.5 V, ±5 V and ±10 V, and is configurable via API functions.

Only the first 12 of 16 channels are available to the user. The ADC input channels are accessed via the front panel ADC SMA (channel 0), and via the SDR connector (channel 0-11). Each ADC channel is sampled at a fixed frequency of 30.3 kHz.

3.1.4 LVDS I/O interface

The LVDS interface provides 3 LVDS inputs, using Texas Instruments DS90LV032A, and 2 LVDS outputs, using Texas Instruments SN65LVDS9638. No supporting logic is implemented on the current version of the FPGA firmware, therefore, this interface is currently not functional.

3.1.5 Backside I/O interface

The backside I/O interface provides connectivity to the Switch Matrix on the FPGA via an SMA connector, with the purpose to connect an external source for the Trigger/SYNC signal, or to make the internal Trigger/SYNC signal available to external instruments.

The connection can be used as input or output. Its connectivity to the Switch Matrix is configured using API functions. The interface requires 5V TTL signals. When used as an output, the SMA signal needs to be connected to a high-Z load. The buffer circuit is the same as for the SMA connector on the Neuropixels PXIe Acquisition module. The I/O signal on OneBox is therefore compatible with the I/O signal of the PXIe Acquisition module. SMA1 on OneBox is compatible with TRIG on the Neuropixels PXIe Acquisition module.

3.1.6 USB interface to PC

The OneBox system communicates to the PC via a USB 3.0 interface. This interface is used for transmitting data acquired by the OneBox system to the PC, and to send configuration commands from the PC to the OneBox system and its connected probes. The minimum USB requirement is USB 3.0.

3.2 Front panel

The front panel is shown in the following picture.

Figure 4: OneBox front panel

The front panel contains:

- One status LED.
- Two USB-C input ports with LEDs
- One SMA DAC connector.
- One SDR connector.
- One SMA ADC connector.

The OneBox system can be used with up to two Neuropixels headstages by connecting them to port 1 & port 2 using the Neuropixels interface cable.

3.2.1 Status LED

The status LED indicates the general status of the OneBox system.

Status LED colors:

- Off: the system is not powered, or the FPGA boot code is not loaded.
- Soft-blinking red: status after switch-on: first-stage boot loader successful, no connection to PC via a USB cable.
- Soft-blinking green: temporary status after USB cable to PC is plugged in, returns to soft-blinking red if no API connection is made after +- 5 seconds. Alternatively, turns to green if API connection is made.
- Green: successful detection of OneBox by the API, warm boot successful
- Red: system disconnected from PC: i.e., USB cable unplugged.
- Blue: system triggered and transmitting data to the PC. After rearming it turns back to green.

- Purple: Buffer overflow.

3.2.2 Port LED

The port LED, next to each USB-C input port, indicates the status of the respective headstage and probe. Neuropixels 1.0 based probes and Neuropixels 2.0 probes have slightly different behaviour.

Neuropixels 1.0 (PRB_1_4_0480_1 and PRB_1_4_0480_1_C) ; Neuropixels 1.0 HD (NP1110) ; Neuropixels 1.0 NHP probes (NP1032 , NP1015 and NP1022), and the 128-channel analog-input headstage (NPNH_HS_30):

- Off: No SerDes clock detected: i.e., headstage without probe plugged in.
- Red: SerDes clock present: i.e., headstage with probe plugged in. Probe not configured by API.
- Green: Probe successfully configured after 'openProbe' API function.
- Blue: Port configured for emulated mode.

Neuropixels 2.0:

- Off: No SerDes clock detected: i.e., no headstage plugged in.
- Red: Headstage with or w/o probe present, not configured by API.
- Green: Probe successfully configured after 'openProbe' API function.
- *Blue: No emulator mode available for Neuropixels 2.0.*

3.2.3 SDR Connector

The SDR connector (female, 3M Interconnect, P/N: 12226-5150-00FR) provides access to the ADC input channels and DAC output channels. The table below gives an overview of the SDR connector pinout.

The SDR connector can be connected to an SDR breakout board (chapter 4.13) using an SDR cable (male to male, 3M Interconnect, P/N: 1SD26-3120-00C-200). These boards provide easy connection to the ADC/DAC channels via BNC connectors.

The SDR connector also contains LVDS signals. These signals are currently not enabled.

Signal	***SDR connector pin number***	***Description***
I/O_0	7	ADCin/DACout Ch0
I/O _1	20	ADCin/DACout Ch1
I/O _2	8	ADCin/DACout Ch2
I/O _3	21	ADCin/DACout Ch3
I/O _4	9	ADCin/DACout Ch4
I/O _5	22	ADCin/DACout Ch5

I/O _6	10	ADCin/DACout Ch6
I/O _7	23	ADCin/DACout Ch7
I/O _8	11	ADCin/DACout Ch8
I/O _9	24	ADCin/DACout Ch9
I/O _10	12	ADCin/DACout Ch10
I/O _11	25	ADCin/DACout Ch11
LVDSIN-0_P	17	Not in use
LVDSIN-0_N	4	Not in use
LVDSIN-1_P	3	Not in use
LVDSIN-1_N	16	Not in use
LVDSIN-2_P	15	Not in use
LVDSIN-2_N	2	Not in use
LVDSOUT-0_P	6	Not in use
LVDSOUT-0_N	19	Not in use
LVDSOUT-1_P	5	Not in use
LVDSOUT-1_N	18	Not in use
VOUT_SDR	1	OneBox 12 V supply
VOUT_SDR	26	OneBox 12 V supply
GND	13	OneBox GND
GND	14	OneBox GND

Table 1: SDR connector pinout.

The internal 12 V supply of the OneBox system is available for the user on the SDR connector. The user can draw maximum 100 mA from this supply. This 12 V output is protected by a 500 mA polyfuse (Bourns, P/N: MF-MSMF050-2).

3.3 Back panel

The back panel is shown in the following picture.

Figure 5: OneBox back panel.

The back panel contains:

- Power switch.
- Power supply connector.
- USB 3.0 type B connector.
- SMA1 connector.

- *Reset button (not in use).*

3.3.1 SMA1

The back panel SMA connector provides a connection to the Switch Matrix on the FPGA (chapter 3.1.5).

3.3.2 USB interface

The USB interface is used for communication with the PC (data transfer and configuration). The USB connector is a 3.0 type B connector.

3.3.3 Power supply connector

The OneBox is delivered with a power supply adapter (Phihong, P/N: PSAA18U-120: 12V, 1A or Phihong, P/N: PPL-18U-120: 12V, 1.6A). The OneBox must be used with the included adapter.

3.4 FPGA functionality

3.4.1 FPGA block diagram

An FPGA schematic overview is shown in the following picture.

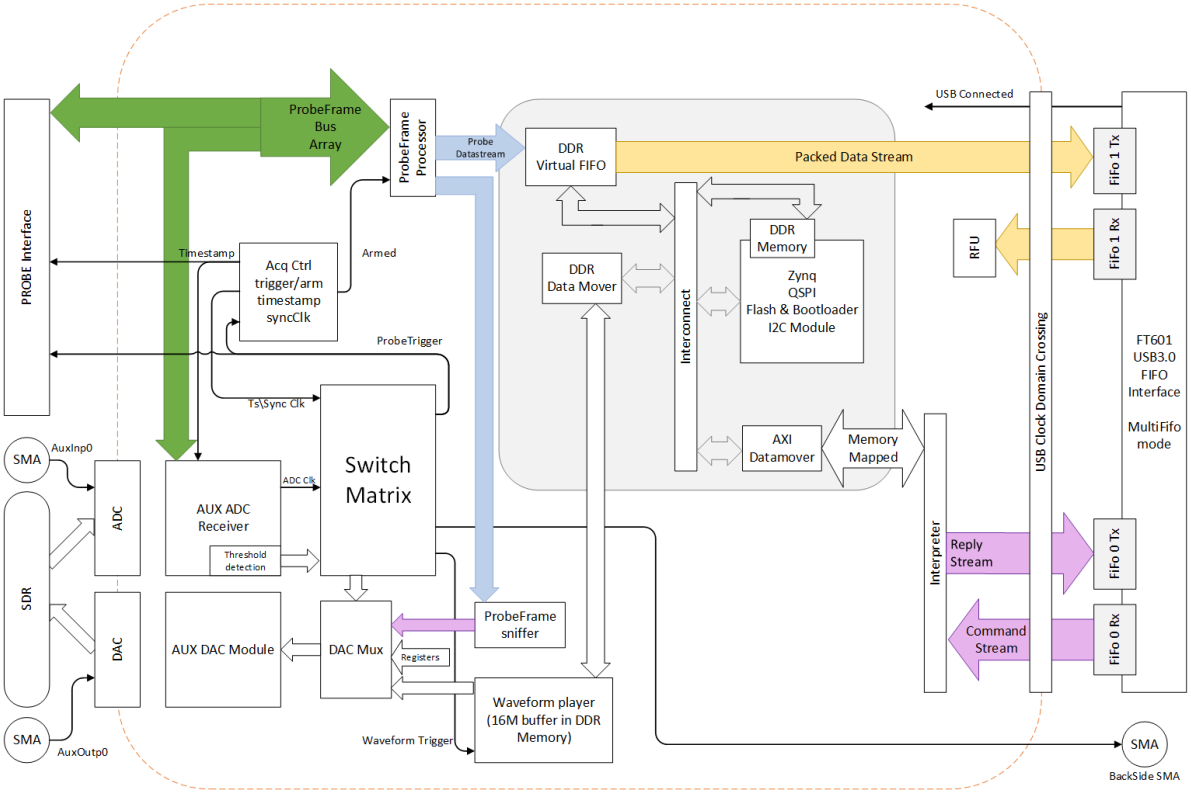

Figure 6: Block diagram FPGA.

3.4.2 ProbeFrame Processor module

The ProbeFrame Processor module handles the acquisition and processing of neural data. The neural data from the probe is transferred over the SerDes link between the headstage and the OneBox. The acquisition control module directly interfaces with the deserializers integrated on the OneBox PCB. The module applies offset and gain correction factors to the neural data.

The module also appends the timestamp counter value and SYNC clock to the neural data packet.

Additionally, the ProbeFrame Processor module acquires and packetizes data packets from the ADC receiver.

The module passes the neural data packets and ADC packets to a FIFO buffer before transmission to the PC over the USB bus.

3.4.3 Acquisition Control module

The Acquisition Control module handles the generation of the timestamp and SYNC clock signal, and arm/trigger signal.

3.4.3.1 Timestamp counter

The timestamp counter generates a 32-bit timestamp. The timestamp clock runs at a frequency of 100 kHz.

When a neural data packet from the probe arrives on the ProbeFrame Processor module, the timestamp counter value is appended to the neural data packet, prior to transmitting the packet to the PC. The same applies to the ADC data packets: the timestamp counter value is appended to the ADC data packet at the time of arrival at the ProbeFrame Processor module, prior to transmitting the packet to the PC.

The timestamp counter is held in reset (value = 0) when the system is in ‘arm’ mode. The counter will start as soon as a trigger signal is detected (chapter 3.4.3.3).

The timestamp counter clock can be routed to the SMA1 connector via the Switch Matrix (chapter 3.4.8).

3.4.3.2 SYNC clock

The Acquisition Control module generates a software configurable SYNC clock. The purpose of the SYNC clock is to synchronize data from multiple sources which are using different time bases.

The period of the SYNC clock can be configured between 2 and 32766 ms, with 2 ms resolution. This corresponds with a frequency between 500 Hz and 0.03 Hz.

The SYNC clock can be routed as an output via the Switch Matrix (chapter 3.4.8) to the DAC and/or SMA1 connector. This is configurable via the API.

It’s also possible to use an external signal as source for the SYNC clock. The external SYNC signal is connected to the Switch Matrix via the SMA1 connector or ADC and comparator. This is configurable via the API.

The ProbeFrame Processor module records the SYNC clock in the STATUS byte as part of the neural data packets and ADC data packets.

The SYNC clock is suppressed when the OneBox system is armed.

3.4.3.3 Trigger / Arm module

The acquisition of neural data and ADC data is started when a trigger signal is received.

Before the trigger, while the system is in 'arm' mode, the incoming neural data and ADC data are discarded, the timestamp counter is set at 0, and all data buffers are empty. When a trigger signal is detected, the system starts the timestamp counter and starts streaming neural data packets and ADC data packets to the PC over the USB interface.

The probe frame sniffer (chapter 3.4.6) remains active while the system is in 'arm' mode.

The source for the trigger signal is selected via the Switch Matrix (chapter 3.4.8) and is configured with API functions. Possible sources for the trigger signal are:

- Software trigger 1 (default).
- Software trigger 2.
- ADC Channel 0 to 11, via comparator circuit (chapter 3.4.4).
- Back panel SMA connector (SMA1)

The trigger edge sensitivity is configurable via the API.

3.4.4 ADC Control

The ADC control module interfaces with the Analog Devices ADC component (chapter 2.1.3).

The ADC input channels are sampled at a fixed clock frequency of 30.3 kHz. The ADC sample clock is generated synchronous with the timestamp counter in the Acquisition Control Module (chapter 3.4.3). The ADC sample clock is asynchronous from the neural probes sample clocks.

The ADC has a configurable input voltage range. There are 3 possible voltage ranges, selectable via an API function.

The ADC Control module contains a configurable comparator circuit on each channel, which can be used for threshold detection. The comparator can be used as a trigger source for the Trigger / Arm module (chapter 3.4.3.3) and WavePlayer (chapter 3.4.7), using the configurable Switch Matrix (chapter 3.4.8). The comparator circuit is configured via the API.

Due to the 30.3 kHz sample rate of the ADC, there is 33 us jitter on the comparator output.

3.4.5 DAC Control

The DAC Control module interfaces with the Analog Devices DAC component (chapter 2.1.2). The DAC can be used for generating analog or digital signals.

The DAC component enables the following functionality, configurable by the API:

1. Output a selectable neural data channel. The neural data channel, as received from the deserializer by the ProbeFrame Processor module, is sent back out on a selectable DAC channel.

2. Generate a waveform that is played from a memory buffer on the OneBox system. The user writes to the memory buffer using API functions. The memory buffer can hold a maximum of 16777215 samples.

3. Generate a DC signal.

4. Output a digital signal from the Switch Matrix (SYNC clock, timestamp clock, ADC comparator outputs).

The DAC component has 12 16-bit outputs. The DAC component is configured by the FPGA via an SPI bus. Therefore, the update rate is defined by the SPI speed, the number of active channels and the DAC settling time. The update rate (sample clock) is configurable via the API. The table below shows which sample frequencies are available, and how many DAC channels can be used for each frequency.

Sample frequency (kHz)	Max. number of active channels
500.00	1
400.00	1
333.33	2
250.00	2
200.00	2
166.67	3
133.33	4
125.00	5
100.00	9
66.67	12
50.00	12
33.33	12
25.00	12
10.00	12

Table 2: DAC sample frequency versus number of active channels.

Any of the 4 DAC functionalities described above count as active channel: a channel used to generate a DC signal also counts as an active channel.

The user can also request sample frequencies which deviate from the frequencies indicated in the table above, but the OneBox system makes an approximation, and returns the real sample frequency to the user. This is configurable via the API.

3.4.6 ProbeFrame Sniffer

The ProbeFrame Sniffer is used to generate the neural data from the probe on a DAC output channel.

The neural data channel which is output via the ProbeFrame Sniffer is configurable via API functions. The user can choose port, probe channel and band (if applicable, only for Neuropixels 1.0 based probes).

The ProbeFrame Sniffer is a block that continuously monitors the neural data stream in the ProbeFrame Processor module. When a sample from the selected neural data channel is received, the ProbeFrame Sniffer transmits it to the selected DAC channel.

The user can select up to 8 neural probe channels to be monitored by the ProbeFrame Sniffer.

The amplitude of the neural data signal output via the DAC depends on a few parameters: ADC resolution and dynamic range of the probe, and resolution and voltage range of the DAC. This results in a gain factor between the recorded neural data signal, as output by the probe, and the DAC output. The gain factor is different for Neuropixels 1.0 based probes and Neuropixels 2.0 probes. The following table gives an overview of the gain parameter for the different probe types.

Probe type	DAC Gain
NP1.0	8.32
NP2.0	10

Table 3: DAC gain factor per probe type

3.4.7 WavePlayer

The WavePlayer allows the user to play an arbitrary waveform on DAC output channel 0. The user writes the waveform from PC to a dedicated memory space on the FPGA module. The WavePlayer module streams the waveform from the memory buffer to the DAC module.

The user can configure how the WavePlayer is started: via a software trigger or a hardware trigger. This is configurable via the Switch Matrix. The user can select between single-shot mode (the waveform is played once) or continuous mode (the waveform is repeated).

The WavePlayer output can connect to only one dedicated DAC channel: channel 0.

3.4.8 Switch Matrix

The Switch Matrix is a configurable matrix through which digital signals on the FPGA can be routed between different modules on the FPGA. Via the Switch Matrix, the user selects which signal triggers the Acquisition Module or the WavePlayer. The source and output for the SYNC clock can be selected. The outputs of the ADC comparators can be routed to be used as a trigger signal or to an output line. The user can select which signal is routed to the DAC channels; in case the DAC channel is configured to generate a digital-like signal.

The following picture shows the Switch Matrix structure.

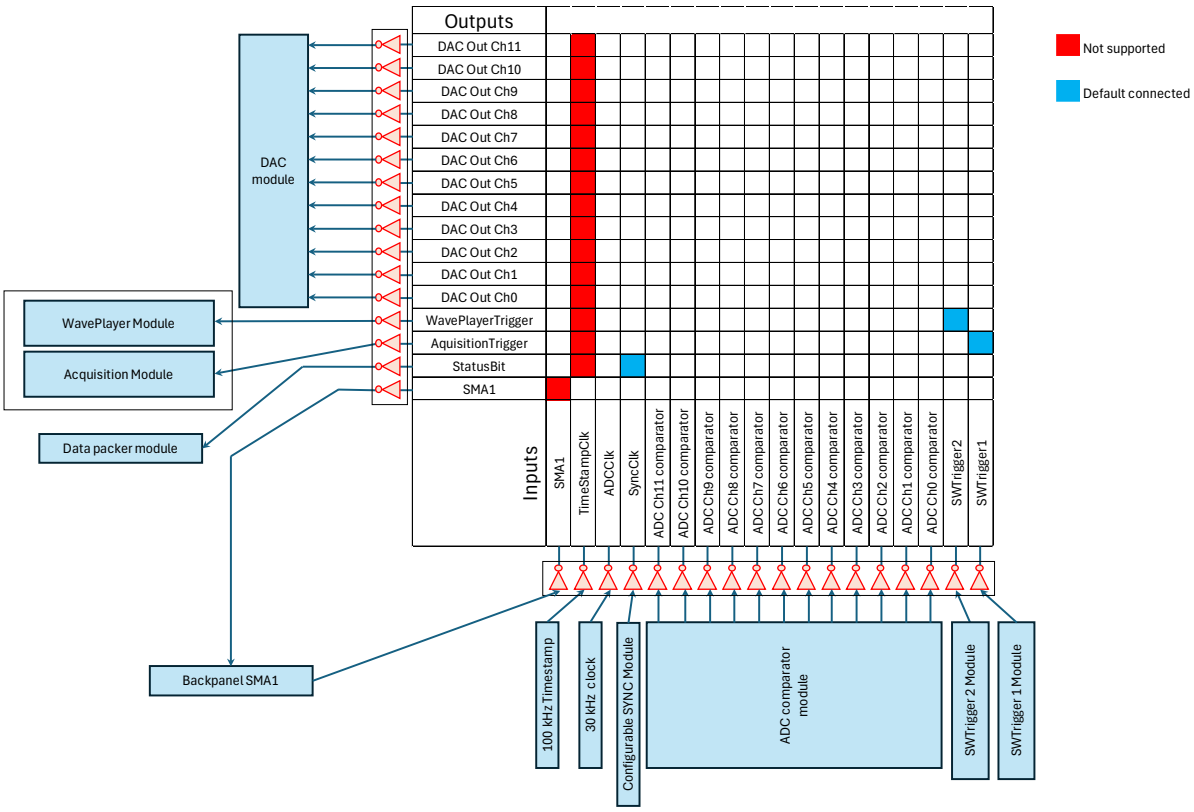

Figure 7: Switch Matrix.

The Switch Matrix outputs are:

- SMA1: the SMA connector on the back panel of the OneBox system. This connector can be used to output any of the input signals of the Switch Matrix. This output is default unconnected.
- StatusBit: a signal connected to this output is stored as bit #6 in the STATUS byte of the neural data packets and ADC data packets. This output is default connected to the internal SYNC clock (input SyncClk).
- AcquisitionTrigger: starts the acquisition of neural and ADC data.
- WavePlayerTrigger: (re)triggers the WavePlayer.
- DAC Out Ch0-11: the 12 channels of the DAC component. Signals routed to these lines are output as a digital signal on the DAC output channel.

Switch Matrix inputs:

- SWTrigger1: the neural data and ADC data acquisition can be started by a software trigger. The software writes to a register on the FPGA. When this occurs, the FPGA generates a 1 ms pulse. This signal is available as an input on the Switch Matrix and can thus be routed to an output of the Switch Matrix. By default, SWTrigger1 is routed to AcquisitionTrigger.
- SWTrigger 2: This register-based software trigger signal has the same behaviour as SWTrigger1 but is by default routed to the WavePlayerTrigger output.

- ADC comparator Ch0-11: each of the 12 ADC channels has a comparator circuit which can be used as digital control signal.

- SyncClk: The output of the internal SYNC clock generator (chapter 3.4.3.2). The SYNC clock is by default connected to the StatusBit output of the Switch Matrix.

- ADCClk: the sample clock (30.3 kHz) of the ADC component.

- TimestampClk: the 100 kHz clock which generates the timestamp counter (chapter 3.4.3). This signal can only be routed to SMA1. When the Acquisition Control module is in 'arm' mode, this clock is suppressed.

- SMA1: the SMA connector on the back panel of the OneBox system. This connector can be used to input any of the input signals of the Switch Matrix, for example acquisition trigger, an external SYNC clock (StatusBit), etcetera.

4 Using the OneBox system

4.1 Location

The OneBox system uses passive cooling to cool down its electronic circuits. The electronic components are thermally connected to the aluminium enclosure. The temperature rise of the enclosure due to the internal heat dissipation is limited. However, it is important not to cover the aluminium enclosure.

4.2 Connecting and switch-on

Please follow the procedure described below to connect the OneBox system to the PC:

1. Plug the power adapter in a wall socket and in the power supply connector on the back panel of the OneBox system.

2. Switch on the OneBox system using the power button on the back panel of the OneBox system. The status LED blinks red.

3. Plug the USB 3.0 cable in the USB connector on the back panel of the OneBox system. Plug the other side of the cable in a **USB 3.x** (SuperSpeed, blue) connector of the PC. The status LED blinks green, and back to red after 5 seconds.

4. The system is now ready for communication with the API, and for connecting headstages and probes.

4.3 Graphical user interface

OneBox can be run with Open Ephys and SpikeGLX. **Please consult the Quick Start Guides via these links:**

- Open Ephys Quick Start Guide
- SpikeGLX Quick Start Guide

4.4 Open OneBox from API

The Neuropixels API functions address the Neuropixels hardware based on a PXIe slot number. Unlike the Neuropixels PXIe modules, the OneBox system is not plugged in a PXIe chassis, and therefore does have a slot number assigned automatically. Therefore, the user can assign a virtual slot number to the OneBox system which is connected to the PC.

The S/N of the OneBox system is printed on a label located on the bottom side of the OneBox enclosure.

It is possible to connect multiple OneBoxes connected to the PC. It is also possible to connect one or more OneBoxes to a PC which is also connected to a PXI chassis. In this case, the user needs to map the OneBox system to a slot number which is not present on the PXI chassis.

4.5 Opening, configuring and using probes

The Neuropixels API provides various functions to control, configure and test the probe, including:

- Selection of recording electrodes, reference inputs, channel gains, and bandwidth.
- Loading of probe-specific configuration files
- Acquiring neural data

These functions are handled by the graphical user interfaces of SpikeGLX or Open Ephys.

4.6 Selecting/generating an acquisition trigger

The acquisition of the neural data and ADC data is started by a trigger signal in the Trigger/Arm module (chapter 3.4.3.3). The user can select the trigger source by configuring the Switch Matrix.

The following trigger sources are available as acquisition start trigger:

- Software trigger 1 (default).
- Software trigger 2.
- ADC comparator ch0-11.
- Back panel SMA connector (SMA1).

These functions are handled by the graphical user interfaces of SpikeGLX or Open Ephys.

4.7 Configuring the SYNC signal

The SYNC signal is recorded in the neural data packets and ADC data packets, as bit #6 of the STATUS byte.

The SYNC clock can either be generated internally in the OneBox system or applied from an external source using the SMA1 connector on the back panel, or an ADC comparator channel. By default, the internal SYNC clock is recorded in the STATUS byte.

The frequency of the internal SYNC clock is configured by the GUI.

It is possible to output the on-board SYNC clock to the SMA1 connector.

The possibility to use external SYNC signals enables sharing of the SYNC signal between multiple OneBoxes and Neuropixels PXIe Acquisition modules.

4.8 Using the ADC

The OneBox system contains 12 ADC channels available for acquiring external signals.

The ADC input channels are available on the SDR connector, on pins which are shared with the DAC output channels (ref. Table 1). Therefore, in case an external signal is connected to an ADC input, it is imperative to disconnect the corresponding DAC output.

When using an SDR signal line for ADC input, make sure to disconnect the corresponding output channel from the DAC.

The GUI can set the input voltage range of the ADC. The GUI can select between ±2.5 V, ±5 V and ±10 V. The default voltage range is ±5 V.

The acquisition of ADC data is done in a similar way as the acquisition of neural data. The transmission of ADC data packets is started by the same trigger signal as the trigger signal selected for the neural data transmission.

The timestamp and STATUS byte are also added to the ADC data packets.

The ADC sample clock is asynchronous to the neural probe clock.

4.9 Configuring the comparator circuit

For each ADC channel, a configurable comparator circuit is implemented on the FPGA. The comparator output signal can be used to detect threshold crossings on the analog input channel of the ADC. Via the Switch Matrix, the comparator output can be used to generate trigger signals and can be output as a digital signal via the SMA1 connector or via the DAC channels.

The threshold levels can be set by the GUI. The threshold levels are shared for all ADC channels.

It is possible to connect the comparator output to for example the acquisition trigger input or WavePlayer trigger input by configuring the Switch Matrix accordingly.

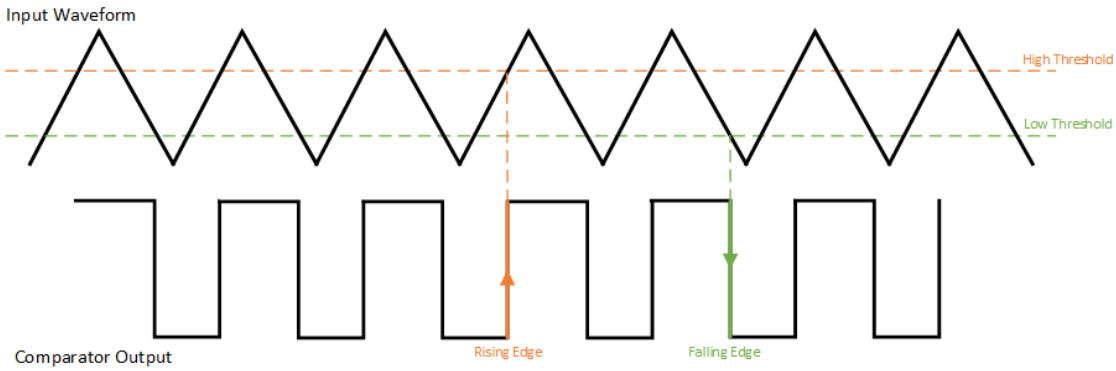

Figure 8: ADC comparator output for triangle wave input.

4.10 Using the DAC

The OneBox system has 12 DAC output channels, for generating analog or digital signals. The channels are accessible from the SDR connector. In addition, channel 0 is also available as a fixed connection on the SMA DAC on the front panel.

The SDR pins are connected to either the DAC or ADC channels via a switch. This switch is controlled by the GUI.

The DAC can either output a DC voltage, a digital output signal from the Switch Matrix, an arbitrary waveform from memory (WavePlayer) or a selectable neural data channel (ProbeSniffer).

4.10.1 DC Output voltage

The GUI can set a fixed output voltage. The available output voltage range is 0 to 5 V.

The GUI sets the selected DAC channel in DC Voltage mode, and disables any previous configuration to digital output, WavePlayer or ProbeSniffer.

4.10.2 Digital output

The DAC can output a digital signal from the Switch Matrix. When connecting a Swich Matrix signal to a DAC channel, that DAC channel is configured for digital output, and a previous configuration to DC voltage, WavePlayer or ProbeSniffer is disabled.

The GUI can set the low and the high levels for each DAC channel. The maximum range is +5 V to -5 V. The default digital level is 0 V (low) – 5 V (high).

4.10.3 WavePlayer

The GUI can write an arbitrary waveform on the on-board memory, which is played by the DAC on channel 0.

4.10.4 ProbeFrame Sniffer

The OneBox system can output a selectable neural data channel on a DAC output channel.

4.11 Switch Matrix configuration

Via the Switch Matrix, the GUI selects which digital signals on the FPGA can be routed between different modules.

A Switch Matrix input line can be connected or disconnected to a Switch Matrix output line using an API function.

It is possible to connect multiple input signals to one output signal, the Switch Matrix uses OR ports.

4.12 Reading the EEPROM

The on-board EEPROM contains the P/N, S/N, version and revision number of the OneBox system. This information can be read out by the GUI.

4.13 Reading the FPGA warm boot code version

The version of FPGA code which is loaded by the API to the FPGA can be read by the GUI.

4.14 SDR breakout board

The SDR breakout board is an accessory board to provide easy access to the ADC and DAC channels. The breakout board connects to the SDR connector on the OneBox front panel using an SDR cable which is shipped together with the OneBox and SDR breakout board.

The SDR cable has orientation marking: one end is marked as ‘Camera Side’. However, the cable can be used in either orientation, the marked cable end can be plugged in the OneBox or breakout board.

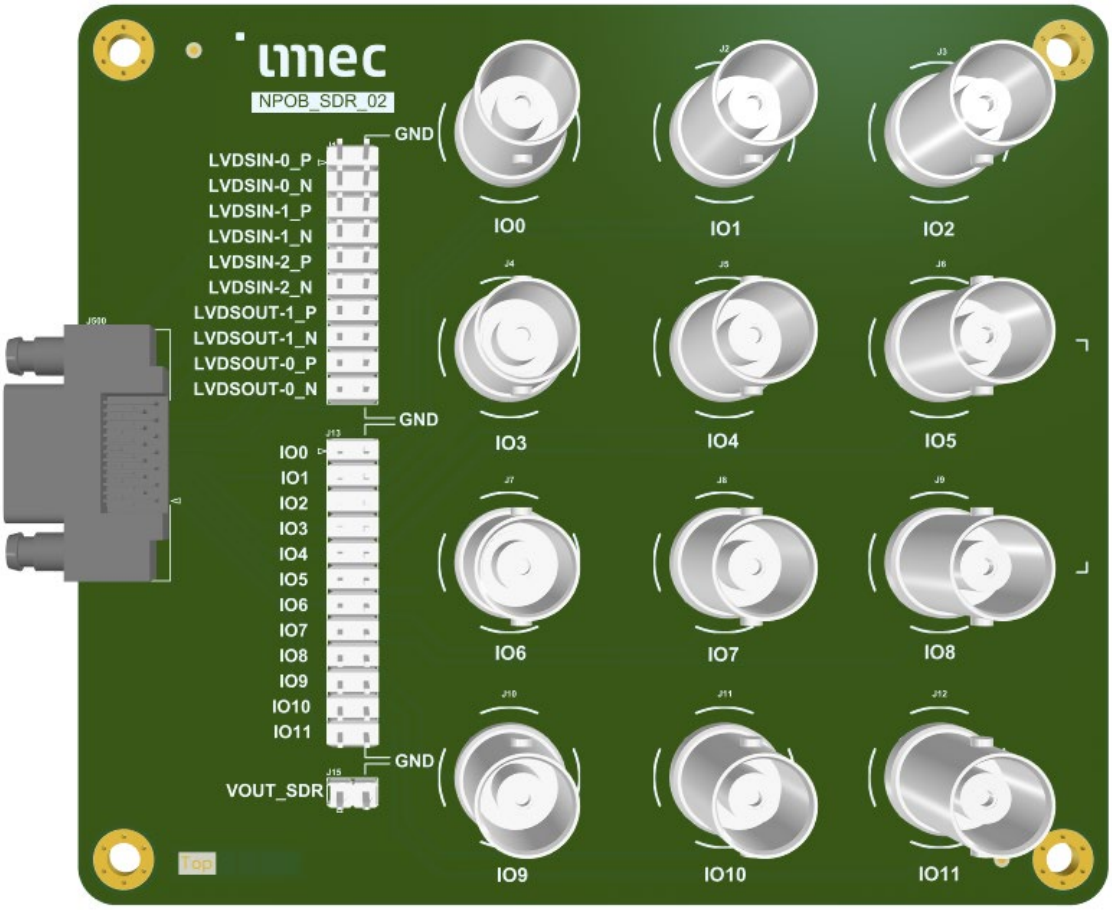

Figure 9: 3D drawing of the SDR breakout board.