# NEUROPIXELS 1.0
# User Manual

February 13, 2020

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# About Neuropixels

The Neuropixels 1.0 neural probe is an advanced silicon CMOS digital integrated microsystem and a tool for neuroscience research. It was developed through a collaboration funded by Howard Hughes Medical Institute (HHMI), Wellcome Trust, Gatsby Charitable Foundation and Allen Institute for Brain Science. Probes were designed, developed and fabricated at imec, Leuven Belgium in collaboration with HHMI Janelia Research Campus, Allen Institute for Brain Science and University College London.

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# List of abbreviations

| | |
|---|---|
| AP | Action Potential. |
| API | Application Programming Interface. |
| ASIC | Application Specific Integrated Circuit. |
| BIST | Built-In Self-Test. |
| CMOS | Complementary Metal-Oxide-Semiconductor. |
| DIW | De-Ionized Water. |
| EEPROM | Electrically Erasable Programmable Read-Only Memory. |
| ESD | Electro-Static Discharge. |
| FPC | Flexible Printed Circuit. |
| FPGA | Field Programmable Gate Array. |
| GND | Ground. |
| HS | Headstage. |
| HST | Headstage Test Dongle. |
| ID | Identification. |
| I/O | Input and/or Output. |
| IPA | Isopropyl Alcohol. |
| LDO | Low-DropOut. |
| LED | Light-Emitting Diode. |
| LFP | Local Field Potential. |
| MSVC | Microsoft Visual C++. |
| MXI | Multisystem eXtension Interface. |
| NI | National Instruments. |
| PBS | Phosphate-Buffered Saline. |
| PCB | Printed Circuit Board. |
| PC | Personal Computer. |
| PCIe | Peripheral Component Interconnect Express. |
| PXIe | PCI eXtensions for Instrumentation express. |
| REF | (External) Reference. |
| RT | Room Temperature. |
| SEM | Scanning Electron Microscope. |
| SMA | Sub-Miniature version A. |
| SMD | Surface-Mount Devices. |
| USB-C | Universal Serial Bus Type-C. |
| ZIF | Zero Insertion Force. |

# Definitions of technical terms

- ASIC: Integrated circuit that contains recording electrodes, amplifiers, multiplexers and digitizers.
- Probe Shank: Implanted part of the probe ASIC (Figure 3).
- Probe Base: Non-implanted part of the probe ASIC (Figure 3).
- Flex: Flexible PCB (or FPC) onto which the probe ASIC and additional passive and active components are mounted (Figure 3). It connects to the HS.
- Control System: System components required to enable control of and data streaming from Neuropixels probes. These entail the headstage, interface cable and PXIe acquisition module.
- Headstage: Miniature board that enables reliable power supply to the probe and is essential for bi-directional data communication from/to the probe (Figure 7).
- Headstage Test Dongle: a small test box (Figure 10) that plugs into the ZIF connector of a headstage. Its purpose is to help verify the functionality of a Headstage.
- Interface Cable: Thin and flexible cable for power and bidirectional data transmission between HS and PXIe acquisition module (Figure 8).
- PXIe Acquisition Module: Custom-made PCB module with two FPGAs for probe configuration, data acquisition and transmission to PC via PCIe interface (Figure 9).
- Port: USB-C plug on the front panel of the PXIe acquisition module. Each front panel contains 4 ports (Figure 9) allowing connection of up to 4 interface cables.
- PXIe Chassis: Houses PXIe modules and connects them with a high-performance backplane that offers timing and synchronization capabilities.
- Driver: The software files that need to be installed on the host PC to enable communication with the Neuropixels control system and to develop custom application software.

# Table of Contents

# 1   About This Manual

This document describes the key features of the Neuropixels 1.0 probe and control system and how to install them prior to use. The Neuropixels hardware consists of:

- The Neuropixels probe.
- The Neuropixels control system which contains:
    - A headstage.
    - An interface cable.
    - A PXIe acquisition module.
- A headstage test dongle.

Even if you have read articles on the Neuropixels 1.0 probes and feel that you are familiar with using the Neuropixels probes we request and encourage you to carefully read the latest version of this *User Manual* to refresh your knowledge and remain up-to-date on possible changes that are relevant to the use of your probes.

If you are unfamiliar with the Neuropixels probes, then it is <u>absolutely essential and imperative</u> that you carefully read the complete *User Manual*.

Please check [www.neuropixels.org](www.neuropixels.org) or [www.neuropixels.info](www.neuropixels.info) for the latest version of this manual.

## 1.1   Related Documentation

The following documents and online resources contain information that you might find helpful as you read this manual:

- Wiki: [https://github.com/cortex-lab/neuropixels/wiki](https://github.com/cortex-lab/neuropixels/wiki).
- Application Software:

    - SpikeGLX: [http://billkarsh.github.io/SpikeGLX/](http://billkarsh.github.io/SpikeGLX/).
    - Open Ephys: [https://open-ephys.atlassian.net/wiki/spaces/OEW/pages/77332482/Neuropixels](https://open-ephys.atlassian.net/wiki/spaces/OEW/pages/77332482/Neuropixels).

- Brochures:

    - Neuropixels 1.0 Probe (available on [www.neuropixels.org](www.neuropixels.org) or [www.neuropixels.info](www.neuropixels.info)).
    - Control System (available on [www.neuropixels.org](www.neuropixels.org) or [www.neuropixels.info](www.neuropixels.info)).

- API Manual (upon request).
- Technical Datasheets (upon request)

    - Neuropixels 1.0 Probe/ASIC Datasheet.
    - System Datasheet.

- Mechanical drawing of the aluminum metal cap (available on [www.neuropixels.org](www.neuropixels.org) or [www.neuropixels.info](www.neuropixels.info)).

# 2 Getting Started

## 2.1 Unpacking and Handling

Upon receiving the Neuropixels probe and control system immediately inspect the shipping boxes and content for damage. In case of damage, please carefully read the included warranty document and follow the instructions.

The probes arrive in black shipping boxes containing black foam inlays. Both the box and foam inlays are manufactured from ESD compliant (antistatic) material. All system components are also delivered in antistatic bags or boxes. It is advised to wear ESD protective equipment when handling the probes and system components. Carefully read the guidelines on probe handling (**Appendix A**), soldering (**Appendix B**) and ESD safety (**Appendix C**).

## 2.2 Hardware & System Requirements

Figure 1 shows the Neuropixels 1.0 probe and control system that can be purchased from imec through www.neuropixels.org or www.neuropixels.info. To get started you need:

- one PXIe acquisition module,
- one data/power interface cable,
- one headstage and
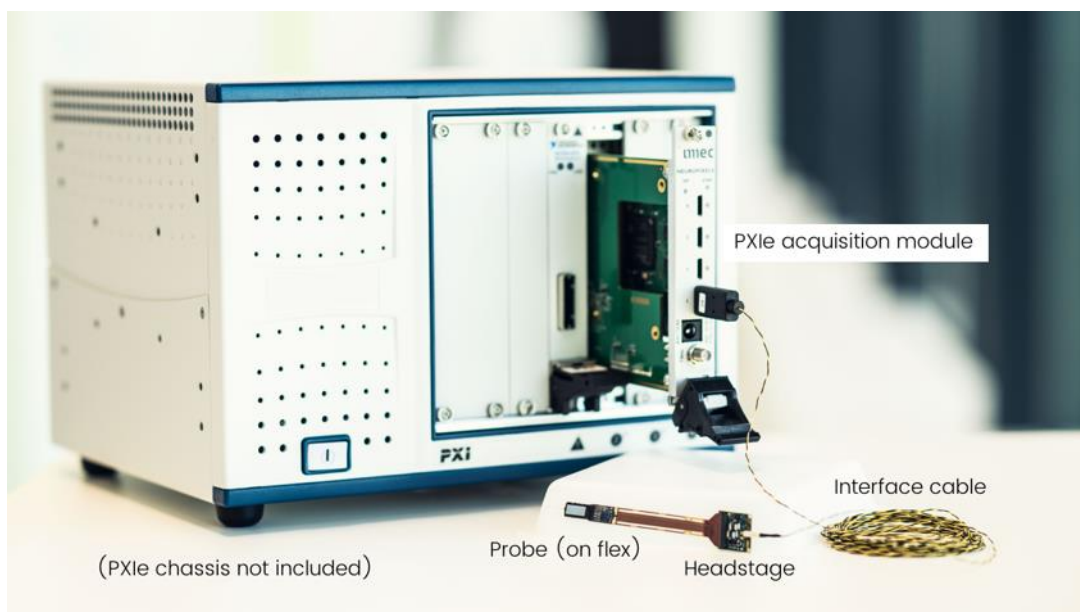- at least one probe.



*Figure 1: Neuropixels 1.0 probe and control system (chassis not included)*

In addition, the PXIe chassis required for using the PXIe acquisition module must be purchased separately from third-party suppliers such as National Instruments (NI), Keysight or Adlink. Below we provide recommendations for PXIe chassis using a remote controller (MXI-Express interface).

For first-time probe users intending to use less than 3 PXIe acquisition modules (or 12 probes) simultaneously, we recommend the following entry-level chassis and remote controller combination:

- PXI-Express chassis: NI PXIe-1071 (4-Slot, Up to 3 GB/s)[1].
- Power cord for chassis[2].
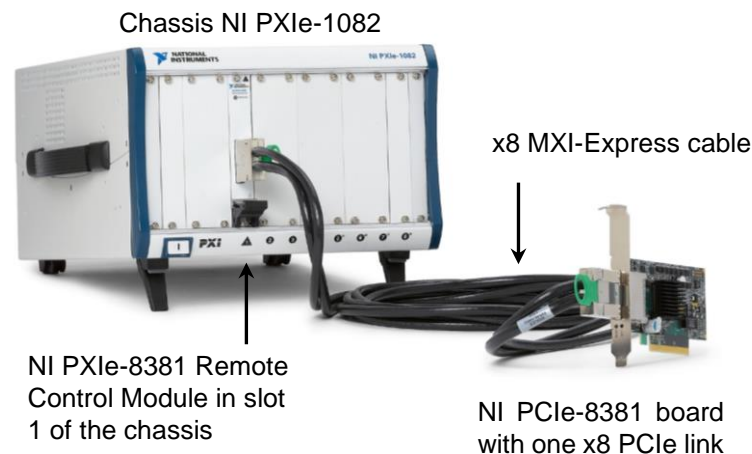- MXI-Express interface: NI PCIe-8381 and PXIe-8381 (Gen 2 x8, 1 Port; incl. one MXI-Express x8 copper cable, 3m)[3].

For more advanced, multi-probe users planning to use 3 or more PXIe acquisition modules simultaneously we recommend:

- PXI-Express chassis: NI PXIe-1082[4].
- Power cord for chassis[5].
- MXI-Express interface: NI PCIe-8381 and PXIe-8381 (Gen 2 x8, 1 Port; incl. one MXI-Express x8 copper cable, 3m)[6].

Chassis NI PXIe-1082



x8 MXI-Express cable

NI PXIe-8381 Remote Control Module in slot 1 of the chassis

NI PCIe-8381 board with one x8 PCIe link

*Figure 2: Recommended PXIe chassis & remote controller combination.*

Other chassis-remote controller combinations are technically possible but have not been tested with Neuropixels probes.

A host PC is needed with:

- Windows 7/8.1/10.
- Dedicated solid state drive for data streaming.
- At least one PCIe slot (Gen 2 x8 or wider) to install the PXIe remote controller.

Please refer to the OpenEphys or SpikeGLX website for exhaustive PC requirements.

Chapter 4 in this *User Manual* contains further instructions on how to install the above hardware.

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[1] NI part number: 781368-01 (http://ohm.ni.com/advisors/pxi/pages/common/intro.xhtml, October 2018)

[2] NI part number: 763000-01 (US), 763067-01 (EU), 763064-01 (UK) (http://ohm.ni.com/advisors/pxi/pages/common/intro.xhtml, October 2018)

[3] NI part number: 782522-01 (http://ohm.ni.com/advisors/pxi/pages/common/intro.xhtml, October 2018)

[4] NI part number: 780321-01 (http://ohm.ni.com/advisors/pxi/pages/common/intro.xhtml, October 2018)

[5] NI part number: 763000-01 (US), 763067-01 (EU), 763064-01 (UK) (http://ohm.ni.com/advisors/pxi/pages/common/intro.xhtml, October 2018)

[6] NI part number: 782522-01 (http://ohm.ni.com/advisors/pxi/pages/common/intro.xhtml, October 2018)

## 2.3   Drivers

To install the Neuropixels PXIe acquisition module you need to download the following PXIe Acquisition Module driver files from the SpikeGLX GitHub site. A separate version is available for Windows 7 and Windows 10.

- *EnPcieDriverWin.inf*
- *EnPcieDriverWin.sys*
- *WdfCoInstaller01009.dll*
- *enpciedriverwin.cat*
- *readme.txt*

Note that the support for windows 7 versions will die out starting January 2020.

Section 4.2.2 of this *User Manual* describes how to install the driver.

## 2.4   Application Software

### 2.4.1   Existing Software

You can acquire data from Neuropixels 1.0 probes with either of two existing software packages: SpikeGLX[7] or Open Ephys[8]. The former is being developed by Bill Karsh at Janelia Research Campus. The Open Ephys GUI is an open-source, plugin-based application for extracellular electrophysiology data acquisition and is being developed by Josh Siegle and Jakob Voigts.

Both packages use the same underlying Neuropixels API to communicate with the probes, so their functionality as far as acquiring data should be identical, though they differ in their online graphical display, interface for modifying probe settings, options for online data processing, and file formats for saving data.

SpikeGLX is distributed with an extensive *User Manual* while Open Ephys has a detailed online *User Documentation* section. To install the software and configure the probes, carefully read these documents and follow the instructions.

### 2.4.2   Developing New Software

If you are interested to develop your own application software, you will need the 32-bit or 64-bit windows *.dll, .lib*, and *.h* files for the API driver. These and the complementary *API Manual* are available upon request. The API is compatible with MSVC and MinGW.

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[7] http://billkarsh.github.io/SpikeGLX/
[8] https://open-ephys.atlassian.net/wiki/spaces/OEW/pages/77332482/Neuropixels

## 2.5 Probe Configuration Files

Probe-specific configuration files will be provided with each probe shipment via the WeTransfer file transfer service to the person listed on the sales order. The provided configuration files must be loaded into software prior to using the probes. These files are <u>essential</u> to correct for CMOS processing-induced deviations of probe performance.

Details on how to load these files into the application software are described in the respective *User Manual* and *User Documentation* of SpikeGLX and Open Ephys.

# 3 Neuropixels Hardware Description

## 3.1 Probe

The Neuropixels 1.0 probe (Figure 3) is a fully-integrated silicon CMOS ASIC with on-chip circuitry for signal conditioning and digitization. The probe features 960 low-impedance TiN recording sites densely tiled along a thin, 10 mm-long, straight shank. The 384 parallel, configurable, low-noise recording channels integrated in the base enable simultaneous, dual-band recording of hundreds of neurons. The electrodes are arranged in a checkerboard layout. Additional specifications are provided in Table 1, Table 2 and Table 3.

*Table 1: Electrode specifications*

| ELECTRODES | |
|---|---|
| NUMBER | 960 |
| PATTERN | Checkerboard |
| PITCH | 16 μm (column), 20 μm (row) (see Figure 3) |
| MATERIAL | Porous TiN |
| SIZE | 12 × 12 μm |
| IMPEDANCE | ~150 kΩ (at 1 kHz in PBS) |
| SELECTIVITY | Local switch under each electrode |

*Table 2: Shank specifications*

| SHANK PROPERTIES AND MATERIALS | |
|---|---|
| NUMBER | 1 |
| WIDTH | 70 μm |
| LENGTH | 10 mm |
| THICKNESS | 24 μm |
| BENDING | ≤100 μm (base to tip) |
| TIP LENGTH | 175 μm |
| TIP SHAPE | Chisel |
| TIP ANGLE | ~20° |
| FRONTSIDE MATERIAL | Silicon nitride ($Si_3N_4$) |
| BACKSIDE MATERIAL | Silicon dioxide ($SiO_2$) |
| SIDEWALL MATERIALS | Silicon (Si), silicon dioxide ($SiO_2$) |

*Table 3: Recording channel specifications*

| RECORDING CHANNELS AND DIGITAL INTERFACE | |
|---|---|
| NUMBER | 384 (dual-band) |
| AP BANDWIDTH | 0.3-10 kHz |
| LFP BANDWIDTH | 0.5-500 Hz |
| AP INPUT-REFERRED NOISE | 5.9 $\mu V_{rms}$ (typical[9]) |
| LFP INPUT-REFERRED NOISE | 9.2 $\mu V_{rms}$ (typical) |
| AP SAMPLING FREQUENCY | 30 kHz |
| LFP SAMPLING FREQUENCY | 2.5 kHz |
| DIFFERENTIAL GAINS | 50-3000 (8 values) |
| CROSSTALK | ≤0.13% (at 1 kHz; typical) |
| INPUT VOLTAGE RANGE | ±5 $mV_{pp}$ |
| ADC RESOLUTION | 10 bits |
| DATA RATE | 163.8 Mb/s |
| POWER CONSUMPTION | ~15 mW (in recording mode; typical) |
| SHANK HEATING | <1°C (in the brain) |

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[9] Process corner

The probe ASIC is packaged (glued and wire-bonded) on a flexible polyimide printed circuit board populated with several SMD components (Figure 3). The components include passives for biasing and decoupling, an IC generating a low-noise reference voltage, and an EEPROM for probe identification. There are multiple input pads for external reference (REF) and ground (GND) on the flex base and along the narrow side arms of the flex cable (Figure 4). These side arms can be cut to length or completely removed when not used.

**NOTE**: *Please be careful when cutting the narrow side arms of the flex. Use a pair of fine, pointed scissors. Avoid any damage to the wider middle section of the flex since this can render the probe non-functional.*

Each probe has a unique identifier code stored on the EEPROM and written on the small label attached to the ZIF area (Figure 5). The acquisition software packages described in Section 2.4.1 automatically read the probe ID stored on the EEPROM.
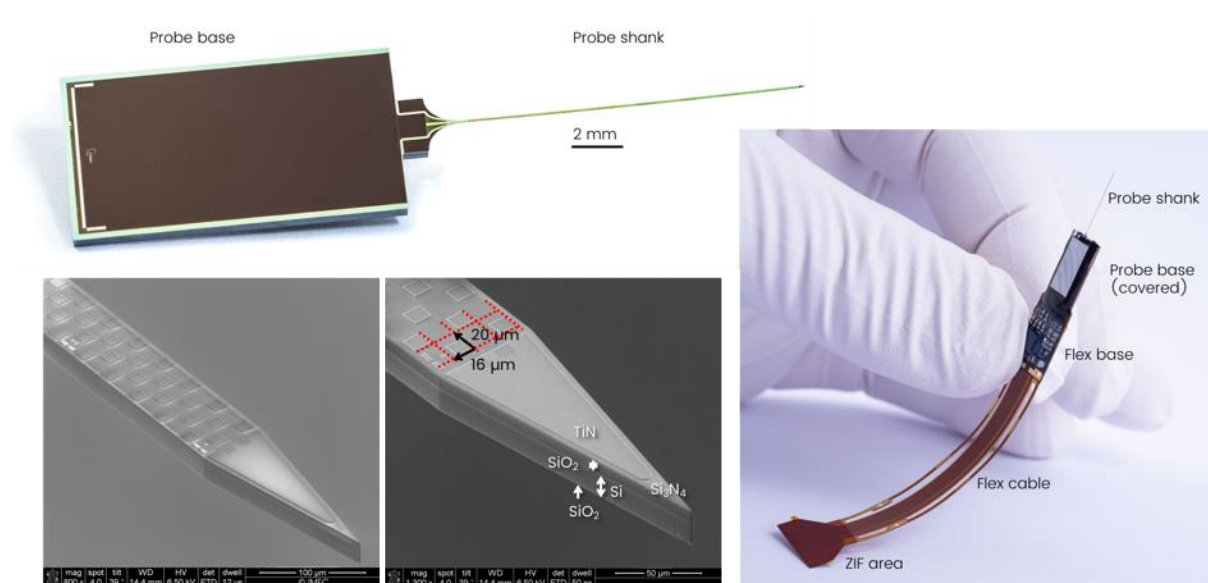


*Figure 3: Top left: Bare die of the Neuropixels probe ASIC. Bottom left: Two SEM images of the probe tip with marked electrode pitch and exposed materials. Right: Packaged probe ASIC with silicon spacer covering the probe base. The SMD components are assembled on the flex base.*
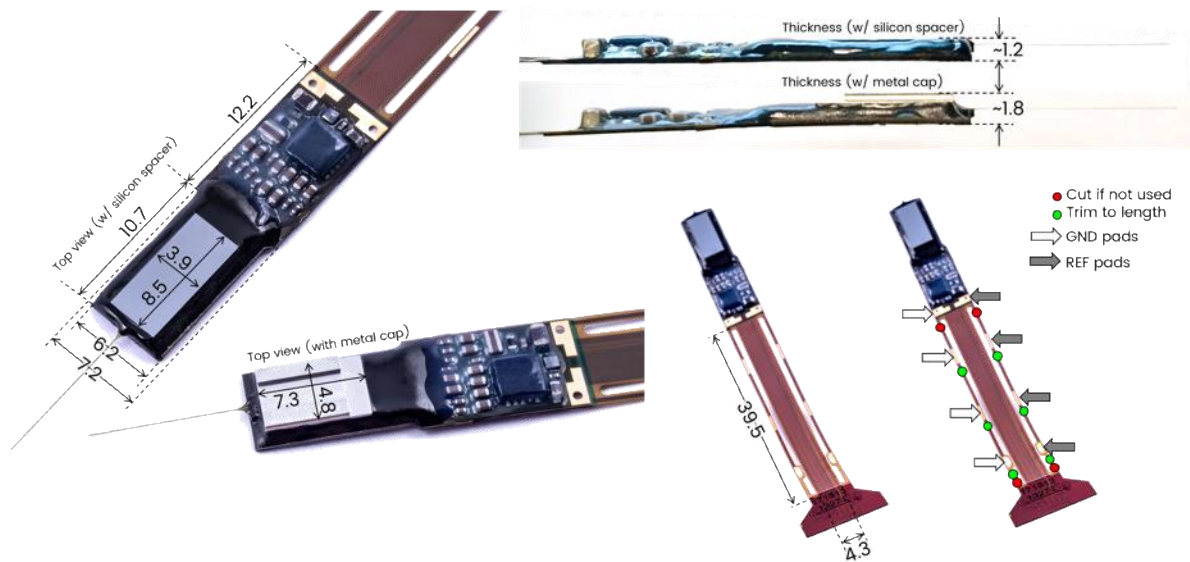
*Figure 4: Top left: Dimensions of a probe package with silicon spacer. Bottom left: Probe package with a metal cap. Bottom center: Dimensions of the probe flex. Top right: Thicknesses of the respective probe packages. Right: Locations of REF/GND pads along the flex. Dimensions are in mm.*
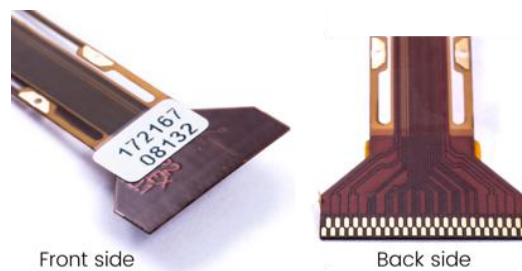


*Figure 5: Left: Label with unique probe ID attached to ZIF area front side. Right: ZIF area back side with metal contact pads.*

The probe base is covered either with a 300-µm-thick silicon spacer (8.5 × 3.9 mm) or aluminum metal cap[10] (7.3 × 4.8 mm) with dedicated dovetail structures (Figure 6). Both probe covers serve primarily as light-shields for the light-sensitive circuits in the probe base but also enable alignment and attachment of compatible stereotactic insertion drives developed amongst others at HHMI Janelia Research Campus.

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[10] Probes with metal cap are available as of June 2019.
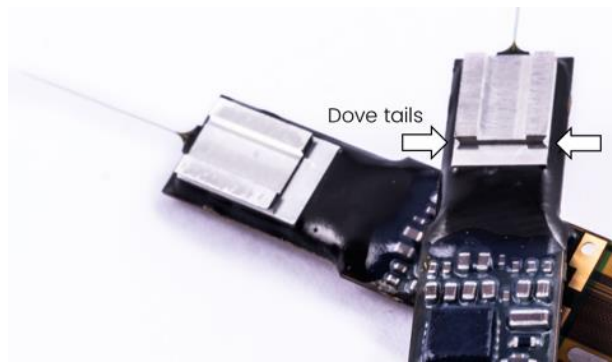
*Figure 6: Probes with stainless-steel cap featuring dedicated dovetail structures.*

A black epoxy (EPO-TEK/H70E) encapsulates the probe perimeter and bond wires. The SMD components are also coated with a conformal, hermetic coating (ELPEGUARD/SL 1307 FLZ-T). The probe package with silicon spacer weighs 400 mg and the one with a metal cap 440 mg. The respective thicknesses at the probe base are ~1.2 mm and ~1.8 mm for the two packages (Figure 4). Table 4 summarizes the package dimensions and properties.

*Table 4: Probe package description*

| PACKAGE DESCRIPTION | |
| --- | --- |
| WIDTH AT PROBE BASE | 6.2 mm |
| WIDTH AT SMD BASE | 7.2 mm |
| WIDTH OF SILICON SPACER | 3.9 mm |
| WIDTH OF METAL CAP | 4.8 mm |
| WIDTH OF FLEX | 4.3 mm |
| LENGTH OF PROBE BASE | 10.7 mm |
| LENGTH OF SMD BASE | 12.2 mm |
| LENGTH OF SILICON SPACER | 8.5 mm |
| LENGTH OF METAL CAP | 7.3 mm |
| LENGTH OF FLEX | 39.5 mm |
| THICKNESS AT PROBE BASE | ~1.2 mm (w/ Si spacer) <br> ~1.8 mm (w/ metal cap) |
| THICKNESS OF FLEX | 80 μm |
| EXTERNAL REFERENCE INPUT | REF (multiple pads along flex) |
| GROUND INPUT | GND (multiple pads along flex) |
| BLACK EPOXY | EPO-TEK / H70E |
| CONFORMAL COATING OF SMD | ELPEGUARD / SL 1307 FLZ-T |
| WEIGHT | 400 mg (w/ Si spacer) <br> 440 mg (w/ metal cap) |

**NOTE**: *Please carefully read and follow the guidelines on soldering (Appendix B) before soldering separate wires to the REF and GND input pads. It is advisable to have prior experience in soldering before soldering to the Neuropixels probes.*

**NOTE**: *Please carefully read and follow the instructions on probe handling (Appendix A) and ESD protection (Appendix C) prior to handling any Neuropixels system components. Familiarize yourself with the probes by first handling and testing dummy probes which can be ordered separately.*

## 3.2  Headstage

The HS (Figure 7) is 16 × 15 mm and weighs 0.9 g. It contains several LDO regulators for power supply, a serializer chip for communication to/from the PXIe acquisition module, and an EEPROM for

identification. A 45-pin FPC ZIF connector with a black latch connects to the probe (Figure 7). A 4-pin Omnetics connector plugs into the 5-m long twisted-pair interface cable (Figure 8).
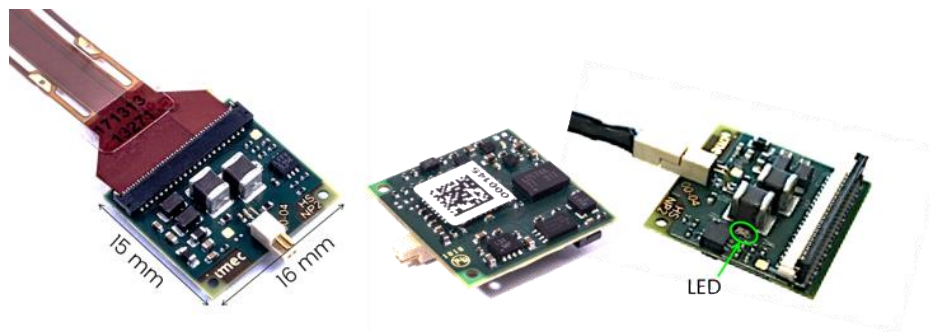


*Figure 7: Left: Top side of a headstage connected to a probe flex. Center: Bottom side of a headstage with unique serial ID. Right: Headstage connected to an interface cable.*

A red status LED (Figure 7) indicates the correct functionality of the headstage. The LED can be enabled and disabled using a dedicated API call. A HS EEPROM contains information on serial number (as printed on the label), part number, PCB version and revision number. Table 5 summarizes the key headstage specifications.

*Table 5: Key headstage specifications*

| HEADSTAGE | |
| --- | --- |
| SIZE | 15 × 16 mm |
| WEIGHT | 0.9 g |
| ZIF CONNECTOR | 45-pin |
| CABLE CONNECTOR | 4-pin (Omnetics) |
| LED INDICATOR | One red LED |
| MECHANICAL FIXTURES | Two mounting holes of 1 mm Ø |

**NOTE**: *Please carefully read and follow the instructions on ESD protection (Appendix C) prior to handling any system components.*

## 3.3  Interface Cable

The Neuropixels single twisted-pair interface cable (Figure 8) provides power from the PXIe acquisition module to the HS and transfers control and neural data to/from the HS. The cable assembly weighs 5 g (excl. USB-C connector) and consists of two 5-m long wire strands each having a diameter of 0.41 mm.



*Figure 8: Twisted-pair interface cable with Omnetics-to-USB-C termination*

The HS side of the cable is terminated with a 4-pin Omnetics connector. The PXIe module side is terminated with a USB-C connector.

*Table 6: Key cable specifications*

| TWISTED-PAIR DATA/POWER CABLE[11] | |
| --- | --- |
| LENGTH | 5 m |
| WEIGHT | 5 g (excl. USB-C connector) |
| DIAMETER | 0.41 × 0.82 mm |
| HEADSTAGE CONNECTOR | 4-pin (Omnetics) |
| PXIE CARD CONNECTOR | USB-C |
| WIRE STRANDS | 1 twisted pair |

**NOTE**: *Avoid repeated sharp bending of the cable (≤ 2 cm bending radius) as this may degrade cable quality and signal integrity. Use the cable only with the Neuropixels PXIe acquisition module; do not plug the cable into any other USB-C port as this may damage the cable.*

## 3.4   PXIe Acquisition Module

The PXIe acquisition module (Figure 9) is a custom-made board with a deserializer chip and two FPGAs[12] for probe configuration, data acquisition and transmission to PC via a PCIe interface. It is compatible with standard PXIe chassis, which must be purchased from other well-known third-party vendors such as NI, Keysight or Adlink. Chassis recommendations are provided in Section 2.2 on page 7.

The module has 4 USB-C input ports thus allowing simultaneous connection and operation of up to 4 probes. Various trigger signals[13] can be configured to synchronize and use multiple PXIe modules and thus probes simultaneously.

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[11] Custom cable assembly.

[12] Xilinx ZYNQ and Xilinx Artix-7

[13] A trigger line switch matrix and configurable sync clock are implemented. Various trigger signals can be programmed: SMA connector, 7 trigger lines on the PXIe bus, user defined data or software trigger. Common trigger for multiple modules and/or external instruments.
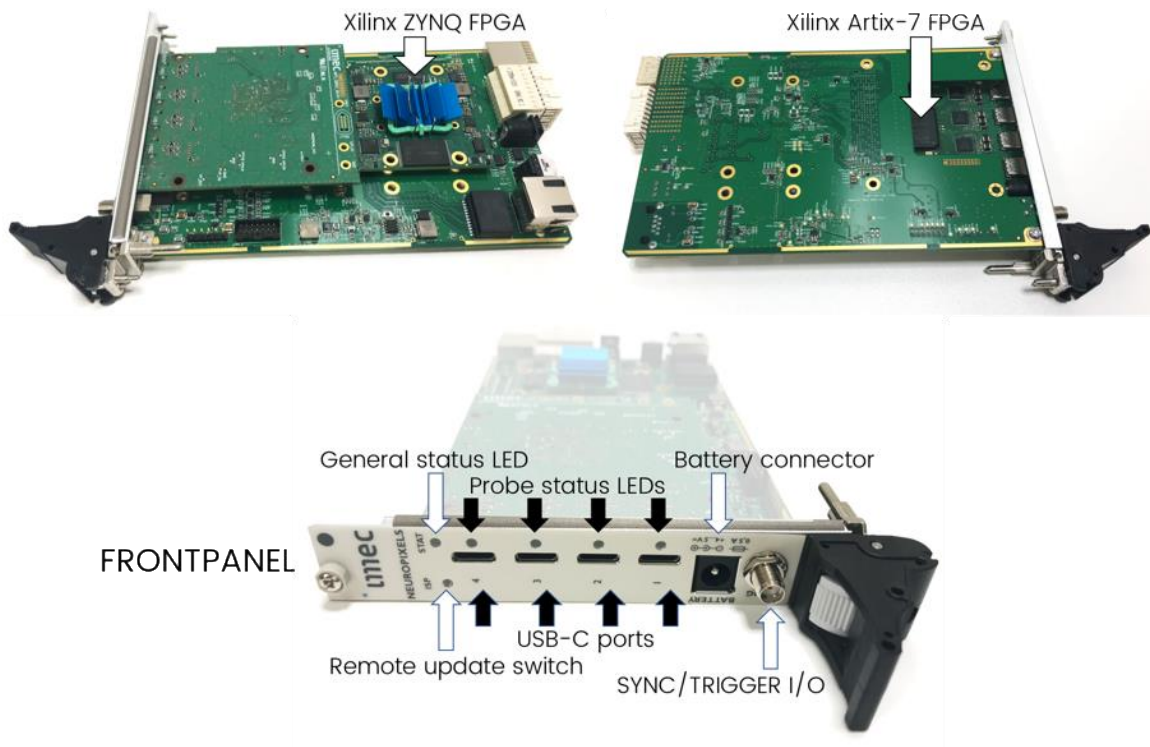
*Figure 9: Top: PXIe acquisition module. Bottom: Front panel of the module.*

The front panel of the PXIe acquisition module (Figure 9, bottom) contains the following connectors and status LEDs:

- Four numbered USB-C ports allow connection of up to 4 probes. Interface cables can plug into the USB-C port in either orientation.
- An LED next to each USB-C port indicates the status of the respective probe and HS:
  o Off: No clock signal (from a probe) detected. This occurs if the power to the port is not enabled, no probe is plugged into the port, or there is a faulty probe, HS, or cable.
  o Red: The probe is powered on but not initialized.
  o Green: The probe is powered on and configured. This is the normal status during operation of the probe.
  o Blinking green: The probe is powered on but not correctly configured.
  o Blue: An internal data emulator on the Artix-7 FPGA is active. The probe data is not used.
- A general status LED indicates the status of the PXIe module:
  o Off: The Artix-7 FPGA is not powered, or the boot code is not loaded successfully.
  o Red: Error status related to ZYNQ FPGA or PXIe bus.
  o Green: The Artix-7 FPGA is powered on and the boot code is loaded, waiting for a start trigger to start transmitting neural data.
  o Blue: The Artix-7 FPGA is triggered and is transmitting data to the ZYNQ FPGA.
  o Purple: Combination of red and blue. Data is not read sufficiently fast by the PC. This indicates data loss.
- A switch used for remote updates of the Artix-7 and ZYNQ FPGA boot codes.
- A battery connector to supply power to the probe and HS. The use of this connector is optional. The hardware automatically detects if an external supply is connected and, if so, switches the port supply from internal system supply to external supply. Connect a 4.0-to-5.0 V battery.
- A SYNC/TRIGGER I/O SMA connector:

o This can serve as an input to connect an external digital trigger signal to start data acquisition, or it can serve as an output to indicate the occurrence of an internal trigger such as a software trigger, a user-defined data trigger, or a trigger from the PXI backplane trigger bus (another PXIe acquisition module or card in the PXIe chassis).

o It can serve as an input for an external SYNC signal, or it can serve as an output for an internal SYNC signal. This SYNC signal is recorded with neural data across all probes connected to the chassis and can be used to align neural data over different probes in time. When used as an output for the internal trigger signal, a 1 ms pulse is generated on the SMA. When used as an input, a pulse with a minimum width of 16 ns must be connected.

o The use and polarity of the SYNC/TRIGGER signal is configured using API functions. The SYNC/TRIGGER line is compatible with 5.0 V logic signals. When used as an output (software trigger or SYNC output), a high impedance load must be connected to the SMA connector to observe the SYNC/TRIGGER output.

An EEPROM contains the serial number, part number, version and revision number of the PXIe acquisition module. While the PXIe module contains hardware provisions for an ethernet connection, neither FPGA code nor API currently support this functionality.

*NOTE: Please carefully read and follow the instructions on ESD protection (Appendix C) prior to handling any system components.*

## 3.5 Headstage Test Dongle

The HS test dongle (HST) is a small test box (Figure 10) that plugs into the HS ZIF connector of a headstage. Its purpose is to help verify the functionality of a HS. This is useful when e.g. neural data seems corrupted or cannot be recorded or when a probe cannot be programmed correctly anymore.



*Figure 10: Headstage test dongle with flex cable that plugs into the ZIF connector of a headstage.*

Verifying the HS functionality is one of the first steps when identifying the root cause(s) for observed failures. The HS tests will be integrated in the application software (Open Ephys, SpikeGLX). In case of failure, the application can provide more detailed information about the exact source of the failure (e.g. power supply, serial data link, clock signal, reset signals, etc. LEDs on the HST indicate status and result of the HS tests. We recommend to always repeat the HS test also with an un-used, good HS to verify that the failure is not related to other system components such as the interface cable.

*NOTE: The API provides several built-in self-tests described in the Troubleshooting Section 5.3. These can be implemented in the application software and help diagnose and debug potential hardware failures along the entire signal chain from ASIC to PC.*

*NOTE: Liquids, metallic particles etc. might cause a short-circuit on the HS. Such short-circuits are detected with the HST, except for 2 specific locations on the HS, which are indicated in yellow on the figure below. If such a short would occur without being detected by the HST, the neural data recorded by the probe will be corrupted on multiple channels.*
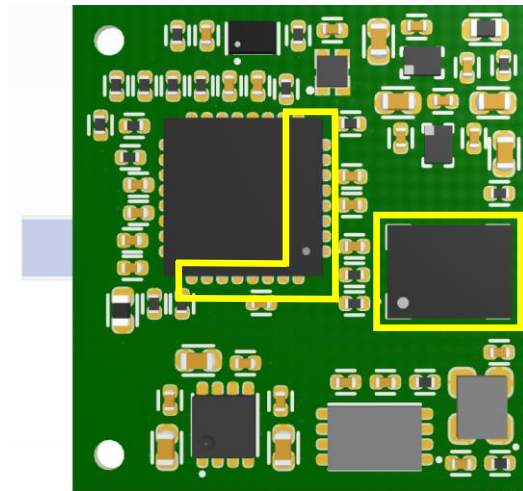


*Figure 11: Locations on the HS in which an electrical short-circuit cannot be detected.*

# 4   Installation and Configuration

This Chapter describes how to install and operate the Neuropixels Control System. Make sure you have the following hardware components available:

- Third-party PXIe chassis + remote controller (see **Section** 2.2 for provider recommendations),
- PC with at least one PCIe slot (Gen 2 x8 or wider) (see Section 2.2 for additional hardware and system requirements; also consult the requirements for the application software you intend to use)
- Neuropixels PXIe acquisition module.

## 4.1   PXIe Chassis and Remote Controller

The first step is to install the third-party remote controller into your PXIe chassis. Here we will provide you with some basic guidelines but do emphasize the need to <u>follow the instructions and safety information described in the user manuals of the chosen PXIe chassis and remote controller provider.</u>

Follow the steps below to install the PXIe-8381 remote controller into the NI PXIe-1071 chassis and the NI PCIe-8381 board into the PC:

1. Power-off the PXIe chassis, but leave the power cable plugged in to ground the chassis.
2. Identify a valid PXIe slot and remove the filler panel. The slot type on the chassis can be identified by symbols next to the slot number, as shown in Figure 12. The PXIe-8381 remote control module must be plugged into the 'PXIe Controller Slot'.

| | |
|---|---|
| ☐ | System Timing Slot |
| ◇ | Star Trigger Slot |
| ◯ | PXI Peripheral Slot |
| ⬤ | PXIe Peripherial Slot |
| ⬤ᴴ | Hybrid Peripheral Slot (accepts PXI and PXIe cards) |
| △ | PXI Controller Slot |
| ▲ | PXIe Controller Slot |
| ◉ | PXIe System Timing Slot or PXIe Peripheral Slot |

*Figure 12: PXIe chassis slot symbols (source: ni.com).*

3. Push the ejector handle down (Figure 13) by pressing the grey button (step 1) on the handle and subsequently pushing the black handle (step 2) down.
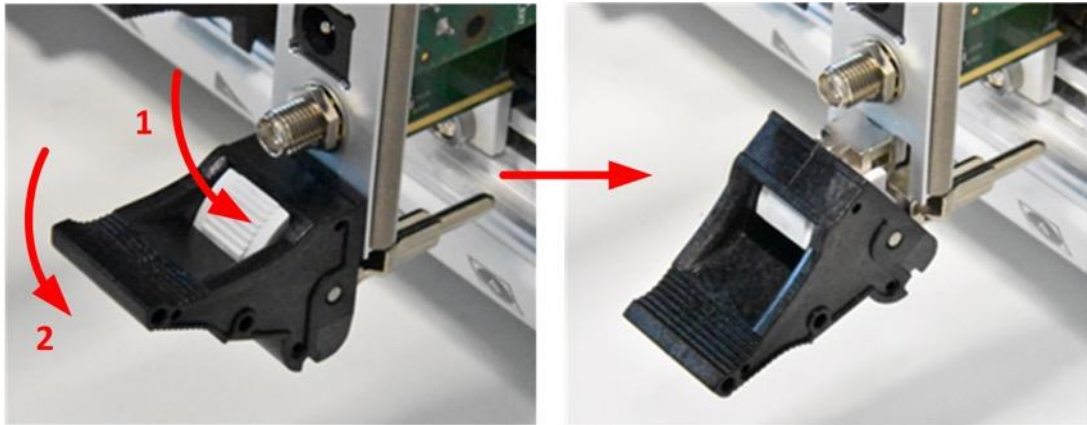
*Figure 13: Push the ejector latch down prior to inserting the module*

4.  Slide the module into the PXIe slot. Observe the correct orientation of the module. When the ejector handle touches the metal rail of the chassis, lift the ejector handle to push the module into the slot for the last few millimeters.
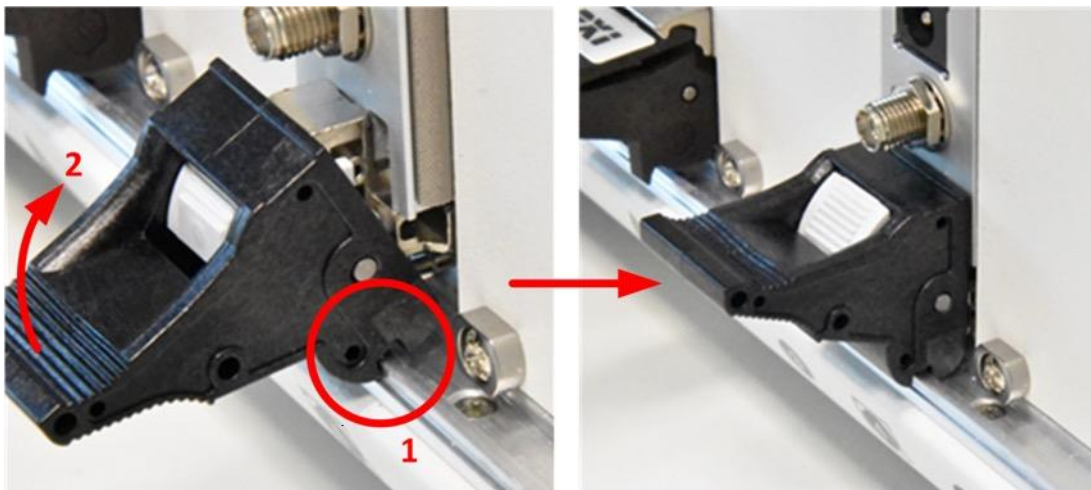


*Figure 14: Push the ejector latch up to plug the BS module into the backplane connectors*

5.  Secure the PXIe module with the mounting screws on the front panel.
6.  Power off and unplug your host computer.
7.  Remove the top cover or access port to the PCIe expansion slots.
8.  Select any available PCIe x8 expansion slot (Figure 15).
9.  Locate and dislodge the metal bracket that covers the cut-out in the back panel of the computer for the slot you have selected.
10. Insert the PCIe-8381 board into the expansion slot (Figure 16).
11. Secure the metal bracket back in place.
12. Replace the computer cover.
13. Connect the MXI-Express x8 cable to both MXI-Express x8 cards. The cables have no polarity, so you can connect either end to either card.

Continue with step 14 further below.

*Figure 15: PCIe x16 slot on the PC motherboard.*



*Figure 16: NI PCIe-8381 board plugged into the PC.*

## 4.2 Neuropixels Hardware

All Neuropixels system hardware is delivered preconfigured by IMEC. No further configuration is required. A remote update procedure is available for the PXIe acquisition module in case an update of the FPGA firmware code is required.

### 4.2.1 PXIe Acquisition Module

Continue with the steps below to install the PXIe acquisition module into the chassis:

14. Ensure the PXIe chassis and host PC are still powered-off.

15. Identify a valid PXIe slot in the chassis and remove the filler panel. The slot type on the chassis can be identified by symbols next to the slot number, as shown in Figure 12. The PXIe acquisition module must be inserted into a 'PXIe Peripheral Slot', 'Hybrid Peripheral Slot' or 'PXIe System Timing Slot'.
16. Follow the same steps 3-5 as above.
17. Power on first the PXIe chassis and then the host computer (in this sequence). The global status LED on your PXIe acquisition module should switch from red to green as shown in Figure 17. The 'LINK' status LED of the remote controller will also turn green.



*Figure 17: Global status LED of the PXIe acquisition module switching from red to green after correct installation.*

### 4.2.2    Drivers

After mounting the PXIe acquisition module into the chassis, install the ZYNQ FPGA driver files that you have downloaded as described in Section  2.3.

*4.2.2.1    Install drivers on Windows 7*

A detailed procedure with screenshots on how to install the driver on a Windows 7 machine is given below.

1. Start the Windows Device Manager with an administrator account. The example in the screenshot below shows the device manager for a chassis with one basestation plugged in, prior to installation. The PXIe acquisition modules show up as **PCI Memory Controller** under **Other devices**.
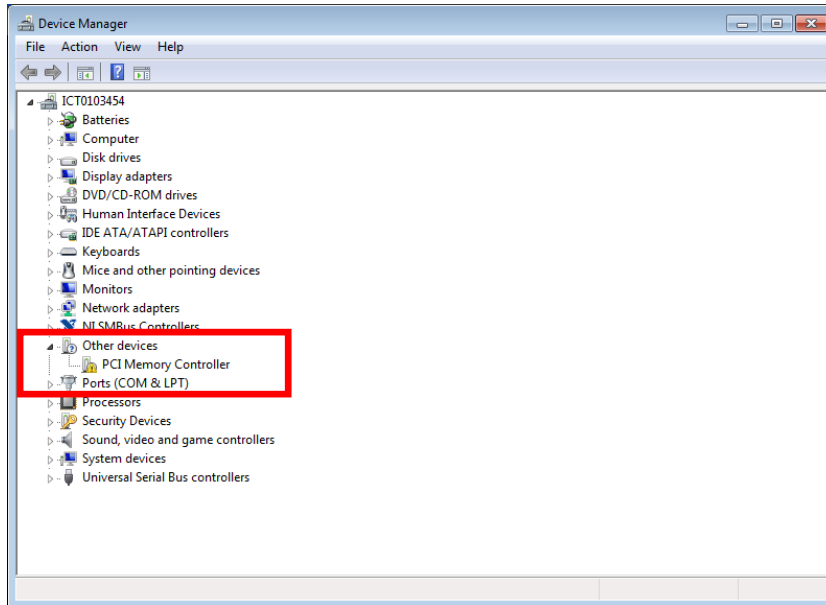
*Figure 18: Windows 7: Device Manager before driver installation.*

2. Right click on 'PCI Memory Controller'. Select Úpdate driver software'.
3. Click 'Browse my computer for driver software'.
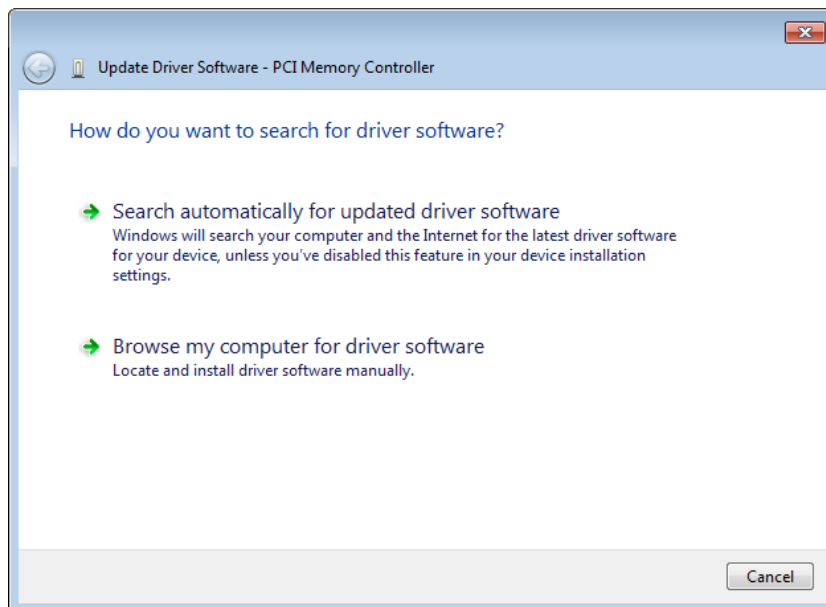


*Figure 19: Windows 7: Install driver.*

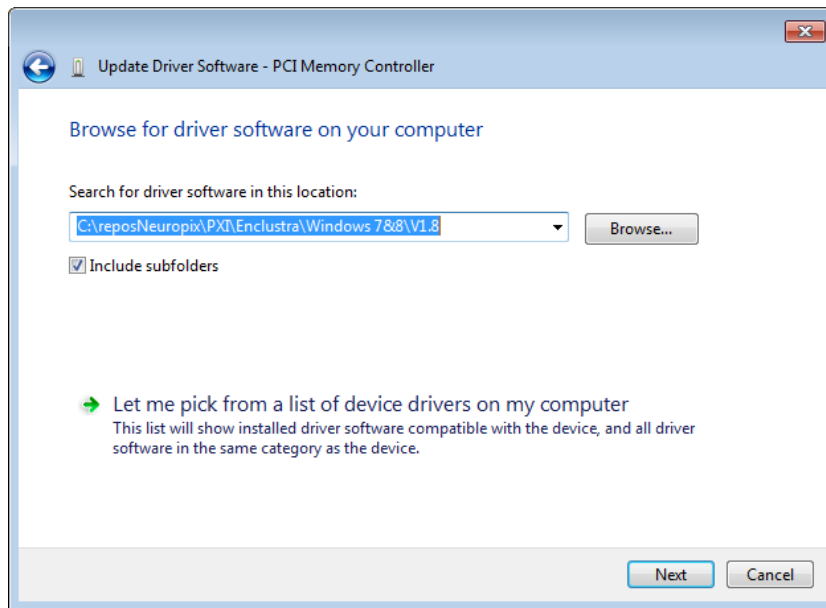4. Browse to the location with the driver files. Click 'Next'.

*Figure 20: Windows 7: Select driver file.*

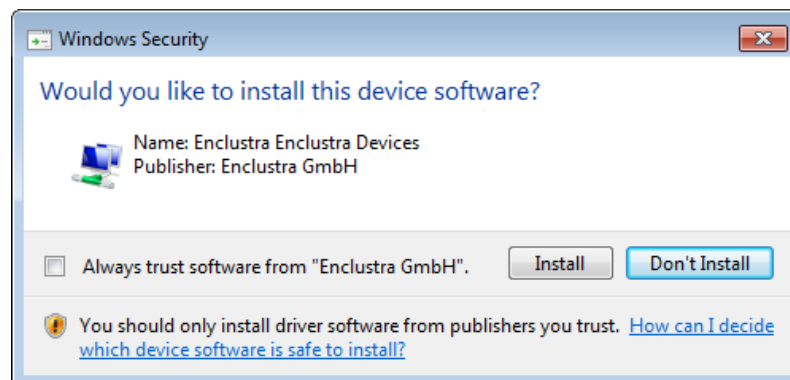5. A warning screen pops up. Click 'Install'.



*Figure 21: Windows 7: Confirm driver installation.*

6. If all goes well, you should get a confirmation that the driver was successfully installed.
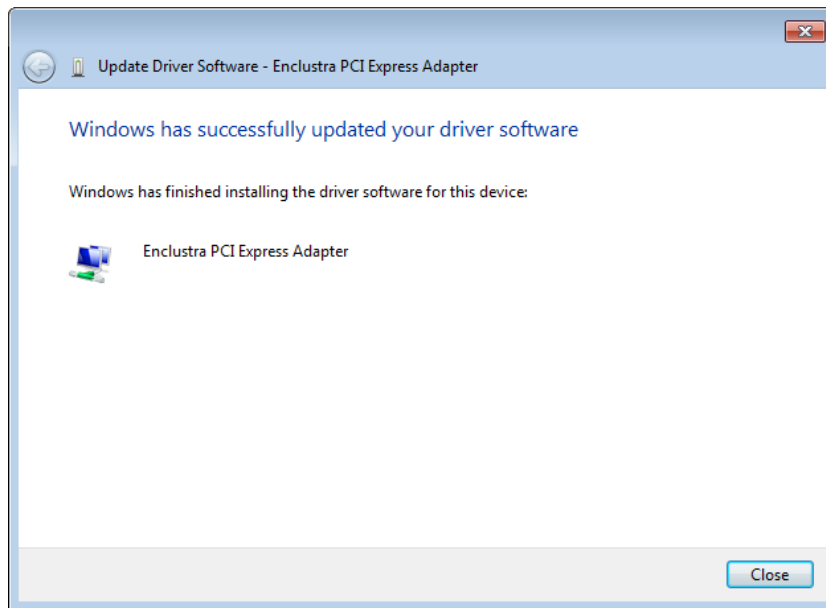
*Figure 22: Windows 7: Successful driver update confirmation.*

7.  Reboot the PC and log in with a normal user account. Check the installation of the driver in the Device Manager. After successful installation, an **Enclustra PCI Express Adapter** shows up in the **Device Manager** under **Enclustra Devices**.
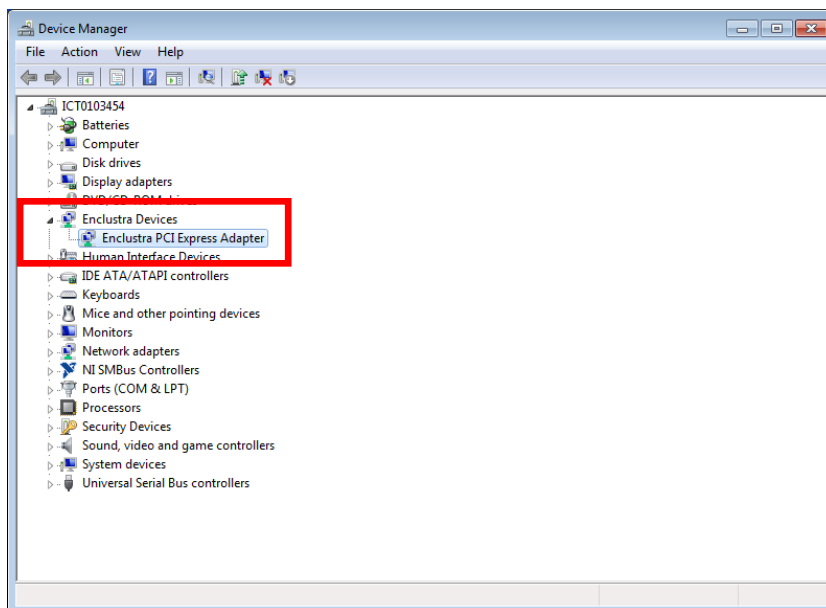


*Figure 23: Windows 7: Device manager after installation.*

A detailed procedure with screenshots on how to install the driver on a Windows 10 machine is given below.

1.  Start the Windows Device Manager with an administrator account. The example in the screenshot below shows the device manager for a chassis with one basestation plugged in,

prior to installation. The PXIe acquisition modules show up as **PCI Memory Controller** under **Other devices**.
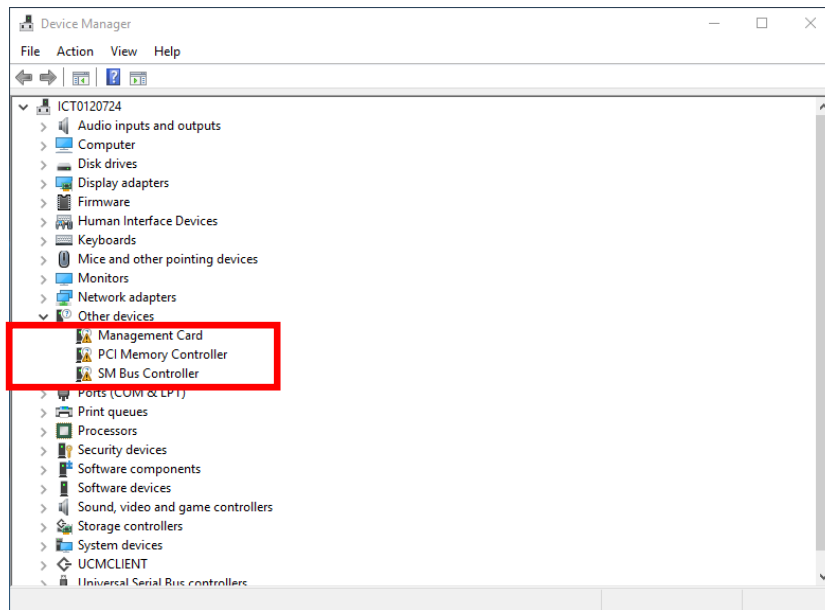


*Figure 24: Windows 10: Device Manager before driver installation.*

2. Right click 'PCI Memory Controller'. Click 'Properties'.
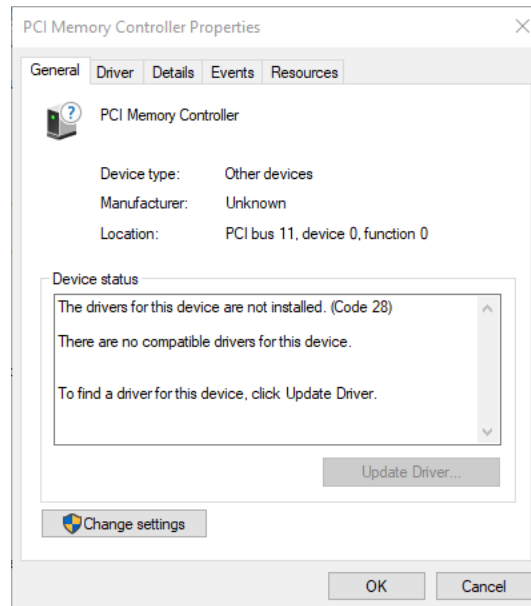3. Click 'Change settings'



*Figure 25: Windows 10: Uninstalled device properties.*
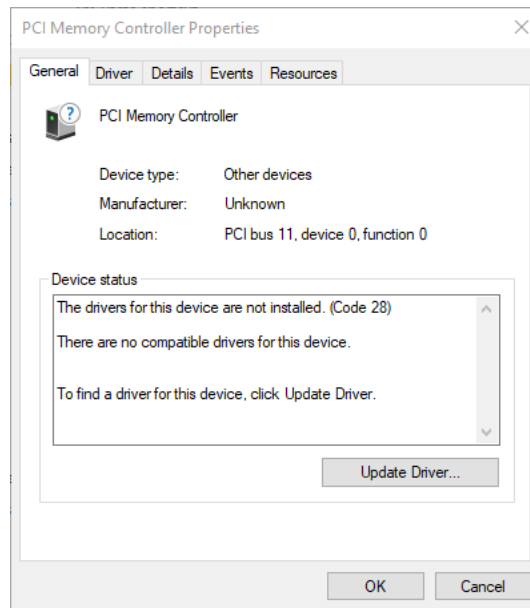
4. Click 'Update Driver...'

*Figure 26: Windows 10: Editable device properties.*
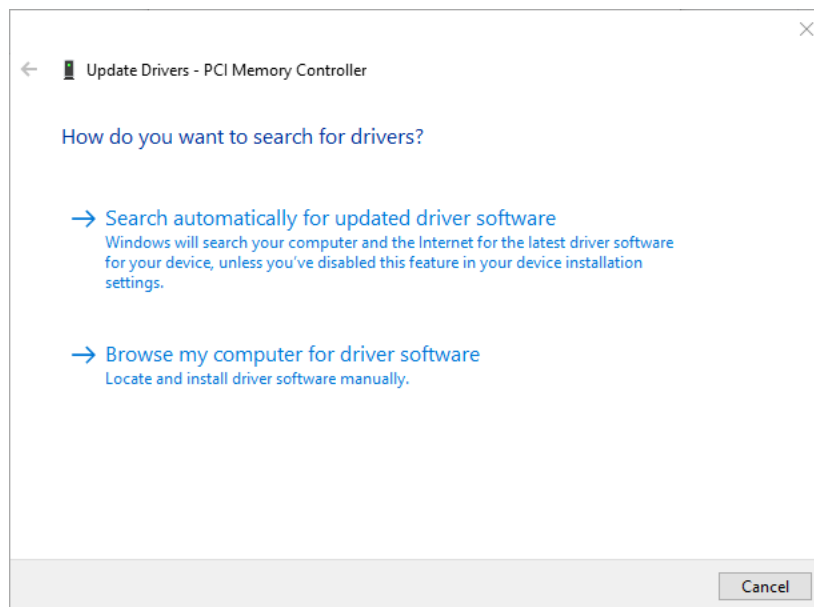
5.  Click 'browse My computer for driver software'



*Figure 27: Windows 10: Install driver.*

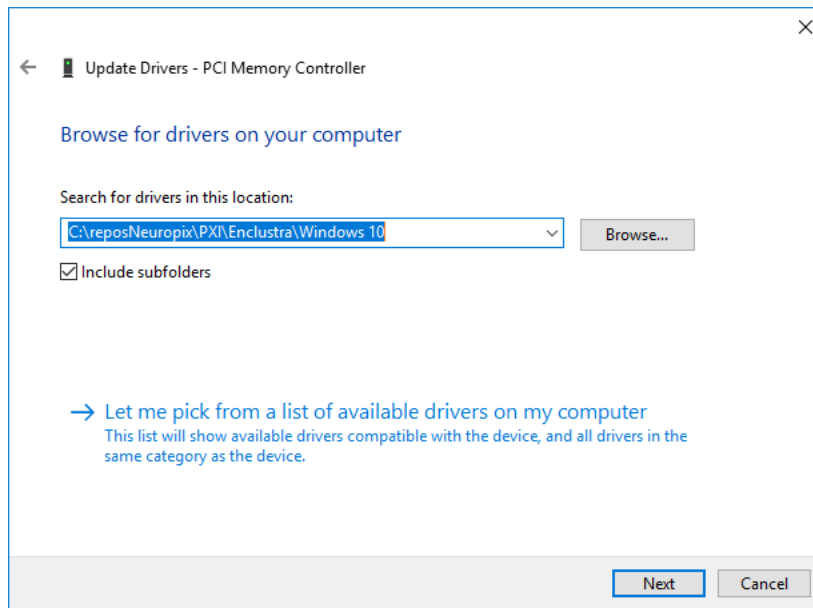6.  Browse to the location with the driver files. Click 'Next'.

*Figure 28: Windows 10: Select driver file.*

7.  If all goes well, you get a screen saying that Windows has successfully updated your driver. Click 'Close'.
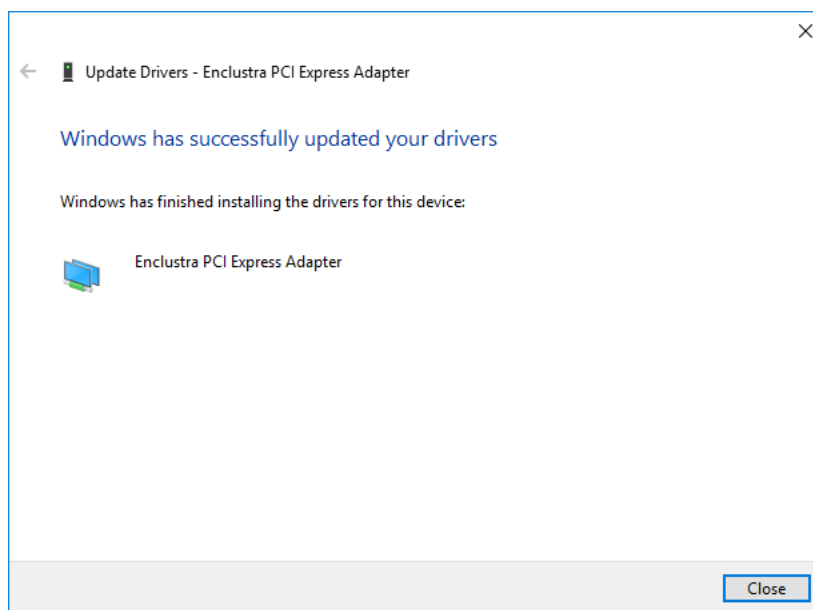


*Figure 29: Windows 10: Successful driver update confirmation.*
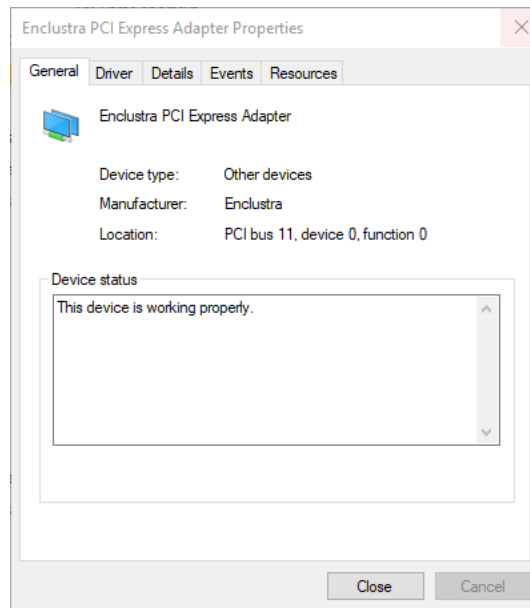
8.  Click 'Close'.

*Figure 30: Windows 10: Device properties after installation.*

9. Reboot the PC and log in with a normal user account. Check the installation of the driver in the Device Manager. After successful installation, an **Enclustra PCI Express Adapter** shows up in the **Device Manager** under **Enclustra Devices**.
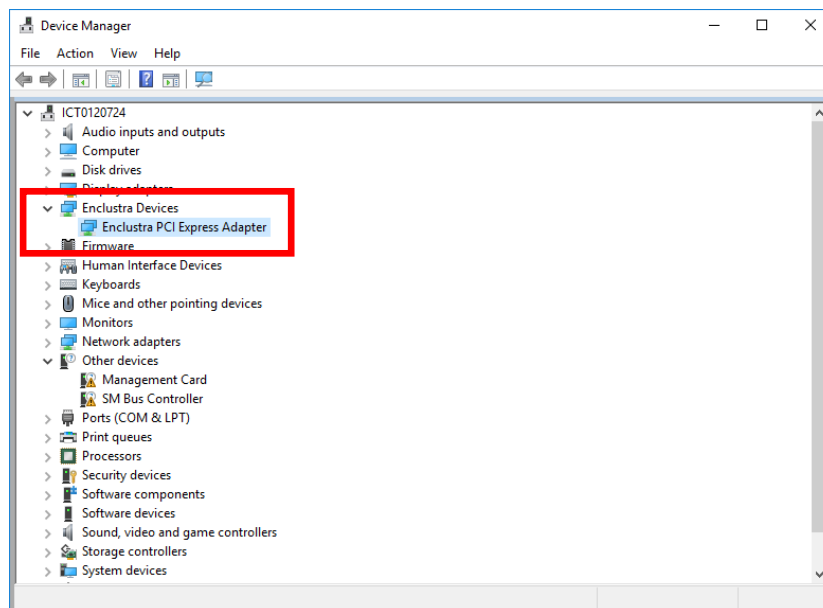


*Figure 31: Windows 10: Device manager after installation.*

On some Windows PCs, the installation of the PXIe Acquisition Module driver may fail and an exclamation mark appears next to **Enclustra PCI Express Adapter** in the **Device Manager** (Figure 32). This occurs if Windows cannot verify the digital signature of the driver[14]. A temporary fix is to disable the driver signature enforcement in the **Windows Startup Settings**.

---

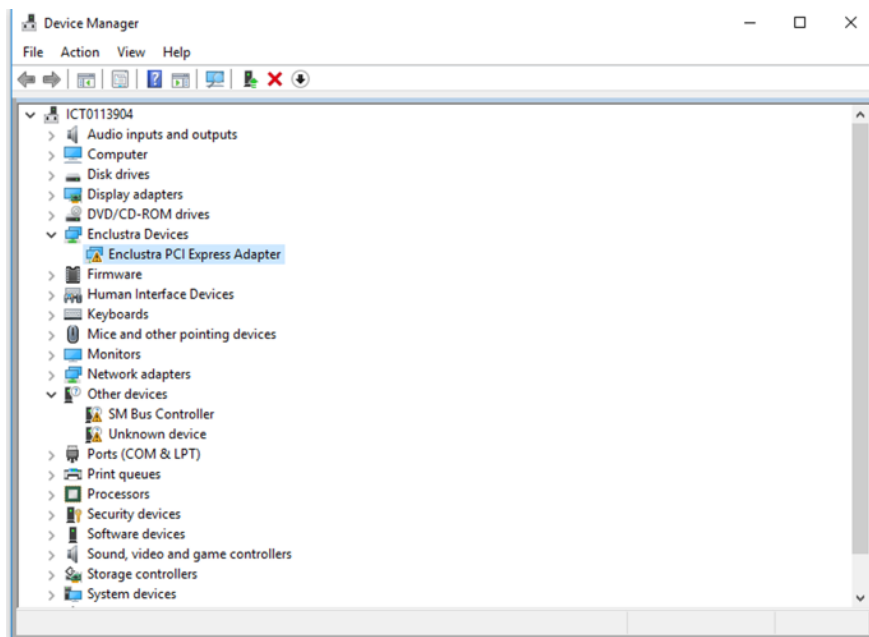[14] Work in progress to enable this feature.

*Figure 32: Unsuccessful PXIe Acquisition Module driver installation.*

In Windows 7, driver signature enforcement can be disabled in the startup settings. To access the startup settings, push the F8 key during boot between BIOS and Windows startup. You need to press the F8 button before the Windows logo appears.

To start Windows 10 in safe mode or get to other startup settings:
1. Select the **Start** button, then choose **Settings**
2. Select **Update & security** > **Recovery**.
3. Under **Advanced startup** select **Restart now**.
4. After your PC restarts to the **Choose an option screen** (step 1 below), select **Troubleshoot** (step 2) > **Advanced options** (step 3) > **Startup Settings** (step 4) > **Restart**.
5. After your PC restarts, select '**7**' or '**F7**', your PC will automatically reboot with the new startup setting.

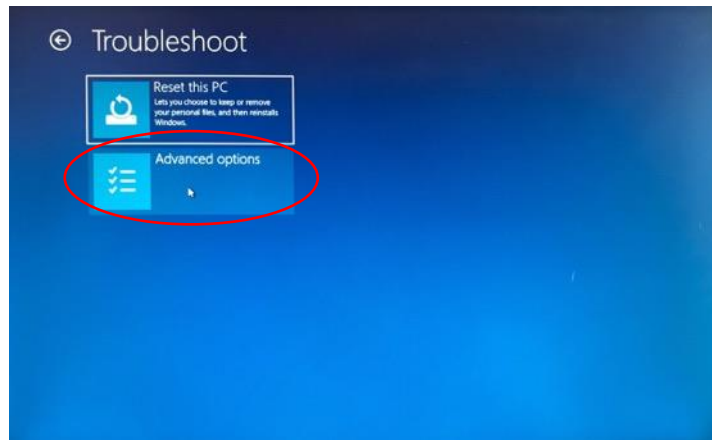Alternatively, you can get to the startup options form the sign-in screen:
1. On the sign-in screen, hold the **Shift** key down while you select **Power** > **Restart** (in the lower-right corner of the screen).
2. After your PC restarts to the **Choose an option** screen, select **Troubleshoot** (step A) > **Advanced options** (Step B) > **Startup Settings** (Step C) > **Restart** (Step D).
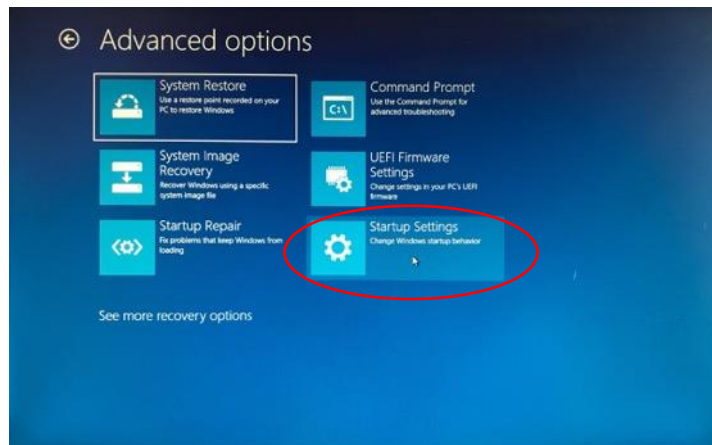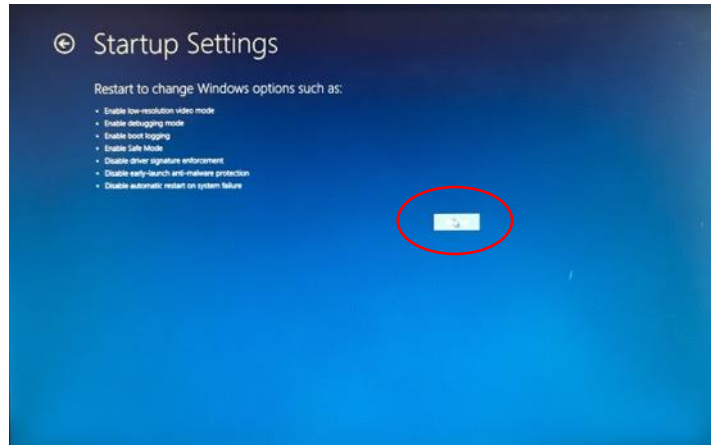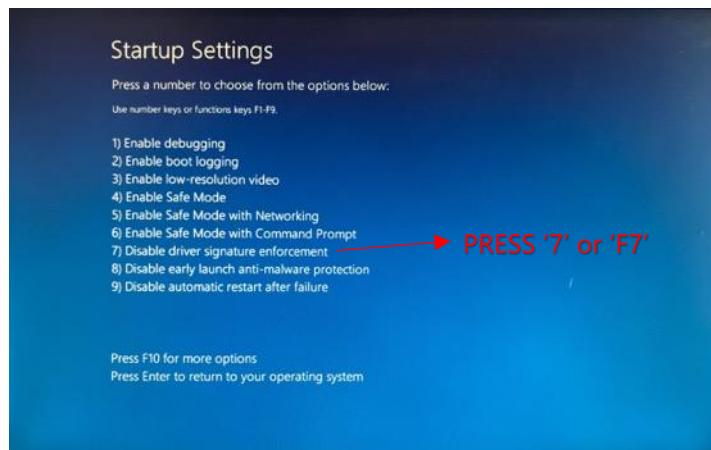
STEP A
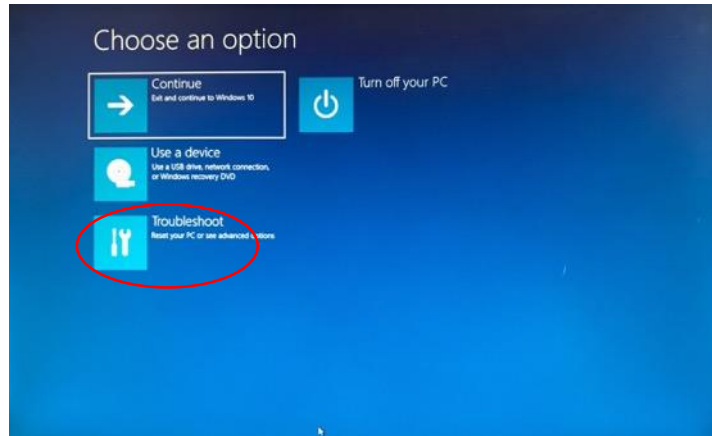


STEP B



STEP C

Step D



3. After your PC restarts, press '**7**' or '**F7**' (Step E), your PC will automatically reboot with the new startup setting.

Step E



An unsuccessful installation of the driver can also be fixed by uninstalling and reinstalling the driver.

4.2.3    Remote FPGA update

The PXIe acquisition module is always shipped with the latest firmware release programmed on the board. However, firmware updates which extend the functionality of the PXIe acquisition module will be released. Updating the firmware on the board can be done with the application software packages SpikeGLX or Open Ephys. However, in case this update procedure would fail, for example due to a power failure of the system during the update process, a recovery procedure needs to be followed:

- If the PXIe chassis has not been switched off after the firmware update procedure has failed, you can simply repeat the update procedure from the application software.
- If the PXIe chassis has been switched off after an unsuccessful firmware update, you need to press and hold the ISP switch on the front panel of the PXIe acquisition module during powering on of the PXIe chassis. You can use a pen to press the switch. Keep the switch pressed for a few seconds, until the STATUS led lights up as green. The update procedure can now be repeated from the application software.

# 5  Using the System

## 5.1  Connecting the System Components

### 5.1.1  Probe to HS

The probe flex connects to the HS via the ZIF connector, as shown in Figure 33. To plug the flex into the HS, gently lift the black latch of the HS ZIF connector (Figure 33, left). If the HS ZIF connector faces up, the gold contacts on the flex cable (Figure 5, right) must face down. Ensure that the flex cable is fully inserted into the HS ZIF connector before closing the connector latch. It is best to close the latch while maintaining slight pressure to keep the flex seated; a good connection is crucial to probe function.
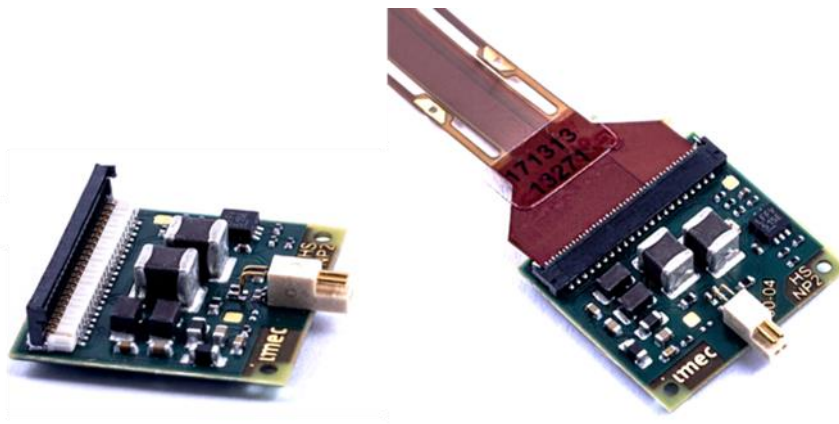


*Figure 33: Connecting the probe flex to the HS*

### 5.1.2  HS to PXIe Acquisition Module

The PXIe side of the interface cable is terminated with a USB-C connector, which is symmetric and can thus be plugged into the PXIe acquisition module in either orientation. The HS side of the cable is terminated with a 4-pin Omnetics connector. This connector is not symmetric and must be plugged into the HS so that the two exposed metal pins mate easily with the two receiving holes (Figure 7 on page 15, right).

*NOTE: Please carefully read and follow the instructions on probe handling (Appendix A) and ESD protection (Appendix C) prior to handling any system components.*

## 5.2  Probe and System Configuration

The Neuropixels API provides various functionalities to control, configure and test the probe and control system, including (but not limited to):

- Selection of recording electrodes, reference inputs, channel gains, and bandwidth.
- Selection of trigger mode.
- Loading of probe-specific configuration files (these files are provided by imec with every probe shipment through a file transfer service).
- Reading of serial numbers, part numbers, hardware versions, and software versions.
- Enabling of BISTs.
- and others.

Most of these functions are already implemented in the application software packages mentioned in Section 2.4.1 and are described in the respective online *User Manual* and *Documentation*.

Below, we will briefly describe the electrode selectivity and reference selection.

### 5.2.1 Electrode Selectivity

Since the shank has 960 electrodes and the base 384 channels, there are 2.5 virtual banks of 384 electrodes in the shank (Figure 34). Therefore, each channel can connect to 2 or 3 electrodes. The connectivity between electrode and channels is given by this formula:

Channel N => Electrode (1+N+384*A), where N = 0:383, A=0:2

For example, channel 0 can be connected to electrode 1, 385 or 769, while channel 199 can connect to electrode 200 and 584 (Table 7).
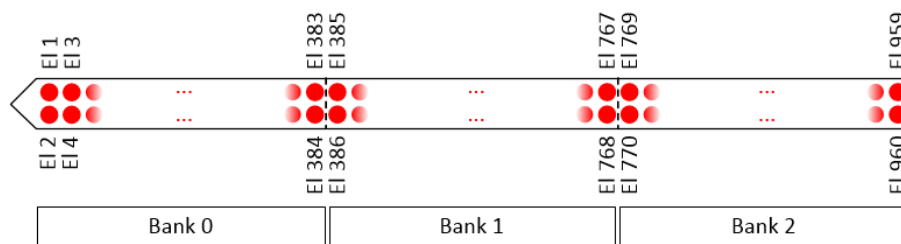


*Figure 34: Electrode bank distribution along the shank*

*Table 7: Electrode-channel mapping*

|  | Bank number 0 | Bank number 1 | Bank number 2 |
|---|---|---|---|
| *Channel* | **Electrode** | **Electrode** | **Electrode** |
| *0* | 1 | 385 | 769 |
| *1* | 2 | 386 | 770 |
| *...* | ... | ... | ... |
| *383* | 384 | 768 | |

### 5.2.2 Reference Selection

Three reference inputs are available for each channel:

- External reference: multiple input pads are located on the probe flex. Separate wires can be soldered to these pads.
- Tip electrode: a large TiN electrode located at the tip of the shank.
- Internal reference: this input can connect to recording electrodes 192, 576 or 960 (i.e. one in each of the three electrode banks)

The reference selection is channel-independent, and each channel can only connect to one of the three reference inputs simultaneously. Moreover, the internal reference can only connect to one of the available three internal electrodes, which are spaced 3.84 mm apart.
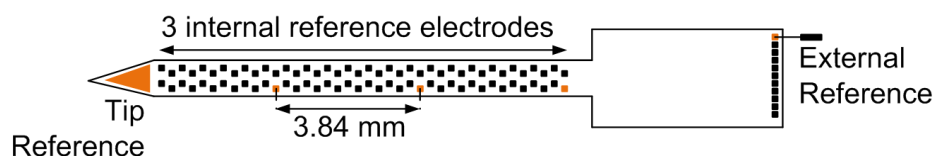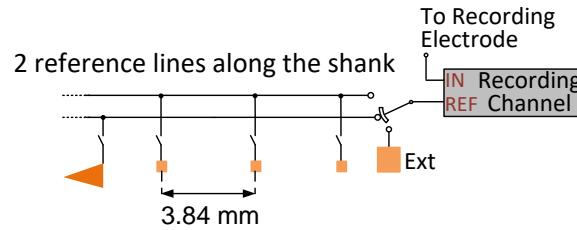
*Figure 35: Reference electrode selectivity.*

## 5.3 Support and Troubleshooting

Neuropixels probes are provided to the neuroscience research community at low cost on a not-for-profit basis. All technical and user support is based on a community support model.

To learn how to use the Neuropixels probe and control system, new users are encouraged to attend one of the regularly organized user workshops or training courses prior to using the probes. Courses are currently offered by University College London through a grant by the Wellcome Trust and generously supported by the Sainsbury-Wellcome Centre.

If your Neuropixels probes appear to malfunction and not perform to specifications, we encourage you to:

- Carefully read this *User Manual*.
- Take advantage of the growing knowledge base shared on various online collaboration platforms: The Neuropixels Slack channel and a GitHub Wiki. In addition, both SpikeGLX and Open Ephys are helpful information sources. A list of available web-based resources is available at www.neuropixels.org.
- As a final option, consult your designated Neuropixels Superuser/Specialist. The original recipient of your Neuropixels probes will be given the contact information of a Neuropixels Superuser/Specialist in your local geography.

In the unfortunate event that your probe is defective and/or non-functional your Neuropixels Superuser/Specialist will confirm this to IMEC directly. IMEC will then contact you and discuss a suitable remedy and process to make sure that you have functional Neuropixels probes. Please wait until an IMEC Neuropixels representative contacts the person who ordered the probes, and please correspond ONLY with the designated person from IMEC who reaches out to you. This will be the fastest and most efficient mechanism for you to resolve issues with your Neuropixels probes. Please do not contact IMEC directly at any of the generic IMEC email contact information addresses.

In the following we describe various tests that you can perform to identify the root cause of observed failures.

### 5.3.1 Visual Inspection

Inspect your probe and system components for visible defects. The probe shank should also be inspected under a microscope to determine possible debris contamination or physical damage such as scratches.

### 5.3.2 Built-In Self-Tests

As a good practice you should start debugging your probe and/or control system by first running the BISTs which must be enabled in the application software. The results will indicate the type and location of possible failures modes. On system level, these tests verify whether all power and data links are

functional and whether data integrity criteria are met. On probe-level, these tests verify the correct programming of and data streaming from the probe ASIC thus assessing functionality and performance of the electrodes and integrated electronics.

### 5.3.3    Headstage Test Dongle

The HST is a small test box (Figure 10) that plugs into the HS ZIF connector of a HS. Its purpose is to help verify the functionality of a HS. This is useful when e.g. neural data seems corrupted or cannot be recorded or when a probe cannot be programmed correctly anymore.

Disconnect your probe from the HS and insert the HST flex into the ZIF connector of your HS. Run the HS tests which are enabled in the application software (Open Ephys, SpikeGLX). In case of failure, the application provides more detailed information about the exact source of the failure (e.g. power supply, serial data link, clock signal, reset signals, etc. LEDs on the HST indicate status and result of the HS tests. We recommend to always repeat the HS test also with an un-used, good HS.

### 5.3.4    Gain and Noise Measurements

The functionality and performance of a probe can also be verified with a simple gain and/or noise measurement in PBS solution. These measurements should be performed after loading the probe configuration files into software.

Gain measurements must be performed using the external REF shorted to GND. This can be achieved by soldering two wires to the respective pads on the probe flex and shorting them to a signal generator's ground (Figure 36). If configured for a nominal gain of 1000 for both AP and LFP channels, a sinusoidal test signal of e.g. 500 $\mu V_{pp}$ and 1.8 kHz or 100 Hz, for AP or LFP band, respectively, can be applied to the PBS using a Pt, stainless steel or Ag|AgCl counter electrode. The resulting mean gain should not deviate >10% from the nominal value and at least 90% of the electrodes should have a gain within 5% of the mean gain. The results can provide qualitative and quantitative information about electrodes and/or channel performance.
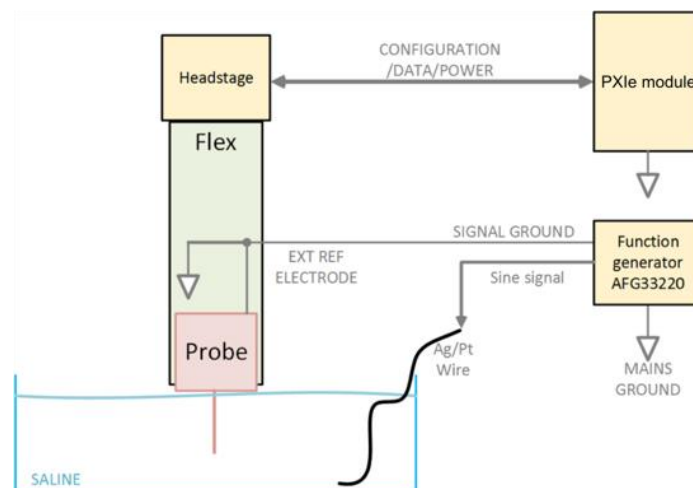


*Figure 36: Setup for gain measurements in PBS.*

Noise measurements should always be performed in a grounded Faraday cage. One can use either an internal REF electrode or the external REF shorted to GND. The reference selection is done via the GUI. The PBS solution must be grounded (Figure 36). During noise measurements, all internal REF electrodes must be immersed in PBS to avoid unwanted noise pick-up and cross-coupling. When using the external REF, the external REF electrode must be grounded via the REF and GND contact pads on the flex.

The nominal gain for both AP and LFP channels should be set to 1000. To obtain the actual input-referred noise, one must divide the measured noise by the actual gain measured above.
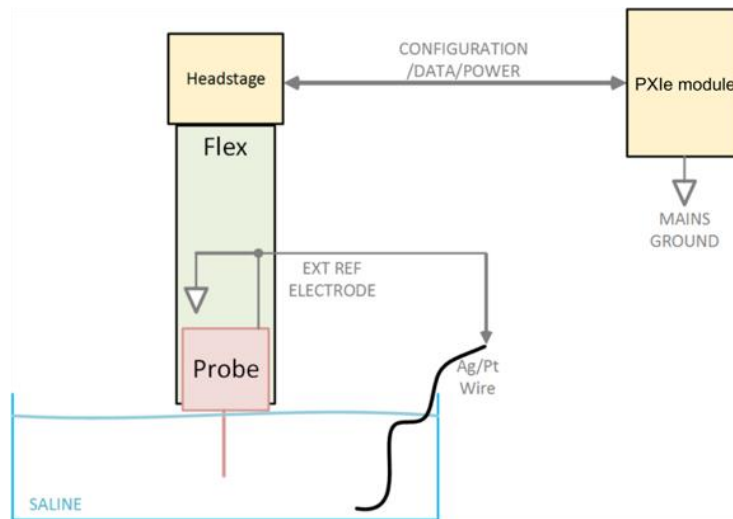


*Figure 37: Setup for noise measurements in PBS.*

# Appendix A    Probe Handling, Cleaning, Storage

Please follow these guidelines to remove the probes from the shipping box:

- Wear gloves to minimize dust and dirt contamination. Work in a clean environment.
- Carefully open the box with the lid pointing away from you. This way the shanks are the farthest from your body. Make sure the lid stays upright.
- Remove the cover foam by lifting it up at the side closest to the lid (Figure 38). The bottom foam has edges to prevent the cover foam touching the probes. By lifting the foam in this orientation, even the corners will never touch the shanks accidentally.
- Up to six probes are shipped in each box.
- We advise to remove probes only from the leftmost non-empty slot to not accidentally touch the other probes.
- Take a pair of ESD-safe tweezers and carefully clamp the base of the probe as shown in Figure 39.
- Hold the ZIF end of the flex with your other hand and keep it straight. Slightly wiggle the base of the probe upwards while pulling the flex along with it. Like this, the flex can smoothly slide out of its slot without getting stuck (Figure 40).
- At all times, keep your eyes on the shank and make sure that it does not touch the foam.
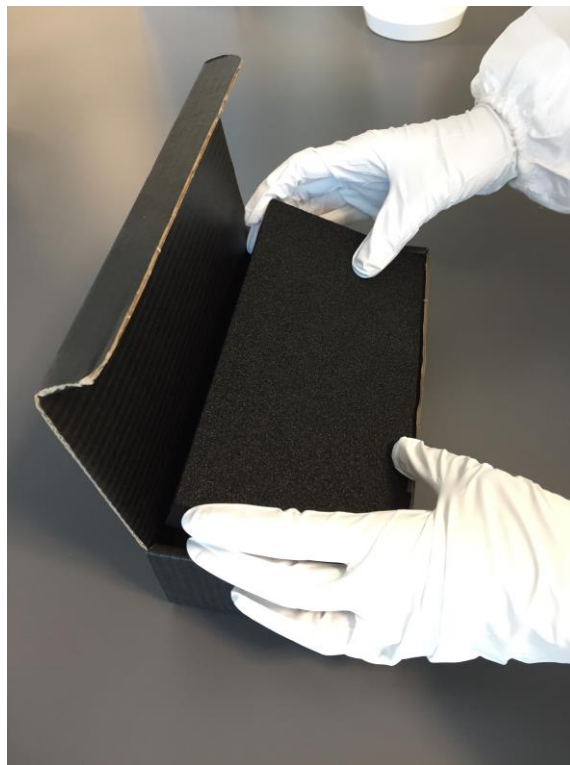


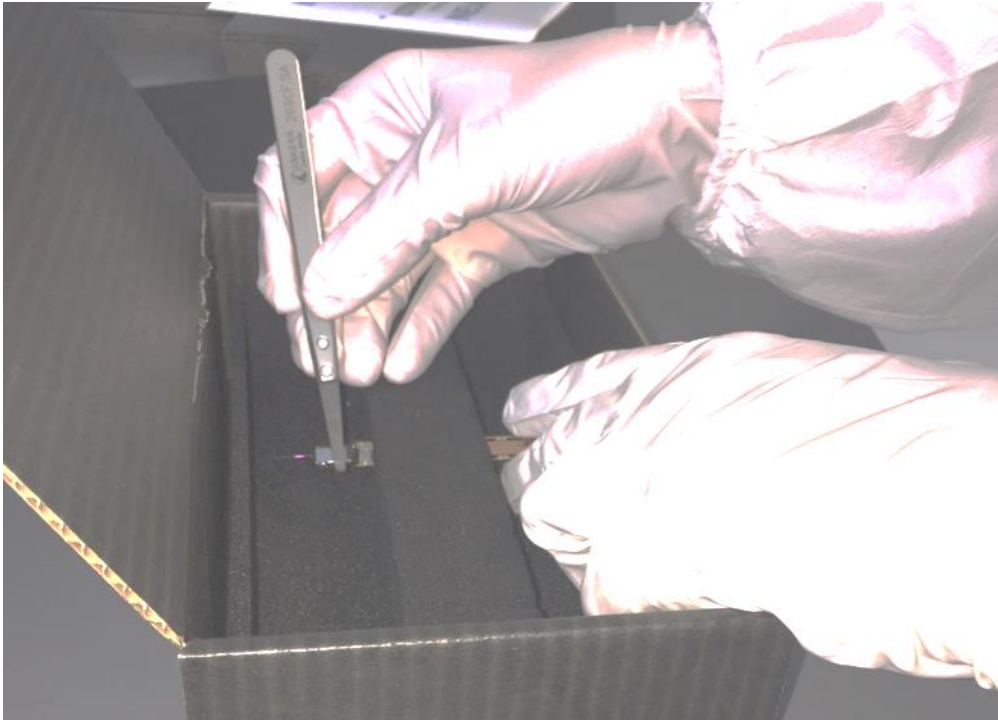*Figure 38: Removing the probe from the shipping box.*

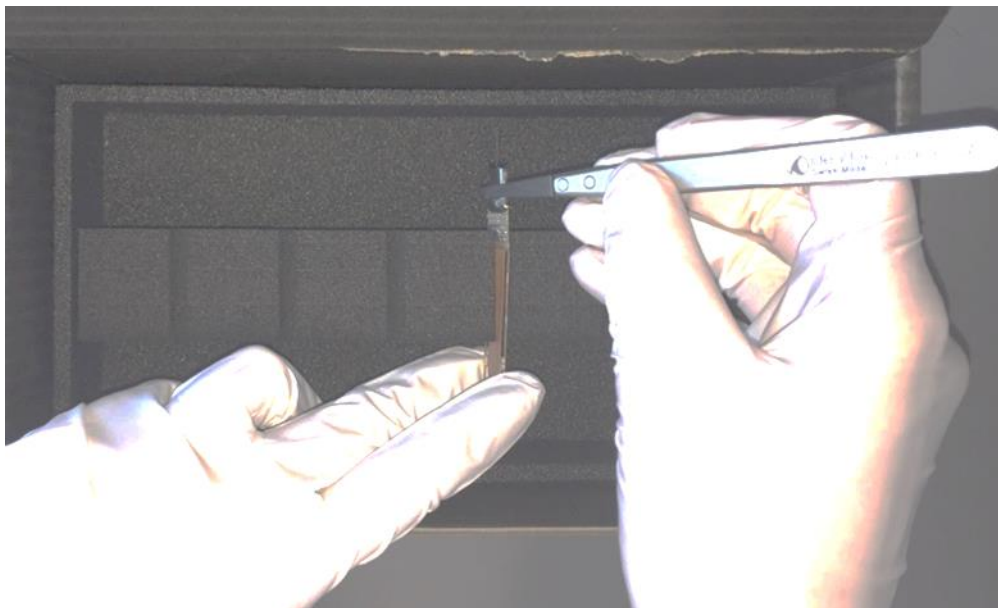*Figure 39: Removing the probe from the shipping box.*


*Figure 40: Removing the probe from the shipping box.*

Please follow these guidelines to ensure mechanical integrity of the fragile shank, electrodes and flex:

- Do not touch the shank with your fingers or other objects.
- Do not subject the probe to vibrations (potential damage of TiN electrodes and shank). Such vibrations could arise e.g. when blow-drying the probe with compressed air or $N_2$ or when subjecting the probe to ultrasound.
- Always work in a clean environment and wear gloves.
- Regularly inspect the probes with an optical microscope to verify that shank and electrodes are undamaged and clean. Color changes/darkening of the TiN can indicate corrosion or other damage. Please report such observations.
- Do not pinch the flex of the probe and maintain a minimum bending radius of 3 mm.

- Store the probes in the black ESD safe shipping boxes at room temperature.

Follow these cleaning guidelines:
- Strong oxidizing agents (acids, bases, $H_2O_2$, etc) and/or elevated temperatures (>100 °C) should be avoided as these may irreversibly deteriorate the TiN electrode impedance and thus noise.
- The following solvents and solutions have been tested and are safe to use with Neuropixels probes (no other organic solvents should be used):
  - Deionized water (DIW)[15] at room temperature
  - Iso-propyl alcohol (IPA)
  - Phosphate buffered saline (PBS) @ pH 7.4 (https://www.sigmaaldrich.com/content/dam/sigma-aldrich/docs/Sigma/Datasheet/pbs1dat.pdf)
  - 25 mM MOPS (3-(N-morpholino)propanesulfonic acid) (http://www.sigmaaldrich.com/catalog/product/sigma/m1254?lang=en&region=BE), 150 mM NaCl, DI water, pH adjusted w/ NaOH and HCl
  - 100 mM MES (2-ethanesulfonic acid) (http://www.sigmaaldrich.com/catalog/product/fluka/69889?lang=en&region=BE), 150 mM NaCl, DI water, pH adjusted w/ NaOH and HCl
  - Tergazyme (http://www.sigmaaldrich.com/catalog/product/aldrich/z273287?lang=en&region=BE )

- When performing experiments in PBS, avoid submersing the electric components into the PBS. While coated with a conformal coating, full hermeticity cannot be guaranteed. Immediately rinse with DIW and IPA and re-test the probe.
- After use in PBS, always rinse the probes (including the electrical components) under a gentle DIW stream or in a beaker for 1-2 minutes followed by IPA rinsing for 1-2 minutes. Do not use a high-pressure water or IPA stream. After IPA rinsing, you can let the probes dry in air. The use of IPA is not mandatory but advised.
- Avoid leaving the probes dry out after removal from PBS. Salt crystals may form on the shank and TiN electrodes that are difficult to remove.
- Always use fresh solutions, i.e. don't use beakers with DIW, IPA, or PBS after prolonged exposure to air (~1/2 day) since dust particles on the liquid surface may irreversible attach to the shank surface when immersed or rinsed with these solutions.
- After in-vivo use, soak the dirty probes in PBS until ready to clean them. Letting the shank dry out makes the cleaning less effective. Follow these cleaning steps:
  - Prepare 1% Tergazyme solution.
  - Soak explanted probes in standard PBS (pH 7.4) until cleaning w/ Tergazyme (to prevent drying out).
  - Immerse probes in Tergazyme solution @ RT (12h soaking on shelf).
  - Thoroughly rinse with DIW (~5 min under gentle DIW stream); if soaking in DIW is used, a brief rinse with DIW should be applied at the end.
  - Rinse the probes with IPA and let dry in air.

Store the probes in the black ESD safe shipping boxes at room temperature.

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[15] Rinsing or prolonged soaking of Neuropixels probes in DIW (pH ≈ 5.7) does not deteriorate the TiN impedance; if anything, the impedance slightly decreases after prolonged soaking (likely due to improved wetting). DIW degassing is not needed.

# Appendix B    Soldering

If the experiment requires a connection to the ground and/or external reference signal, the user can make use of the two GND and REF arms which are part of the probe flex. In case these arms are not usable as such, the user can extend or replace these by soldering wires to the provided solder pads on the flex. Four solder pads are available for both GND and REF connection. These solder pads are reinforced with blind vias to prevent peel off of the solder pads from the flex.

A well-maintained solder iron makes soldering to the probe much easier. Below are some general guidelines to keep your solder tips in good condition:

- Set the temperature of the solder iron to the minimum required for the application.
- Apply some solder to the solder tip before switching off. This prevents corrosion to the tip.
- Switch off the solder station or unplug the solder iron from the station when not in use.
- Replace the tip when the solder wire does no longer melt on the very tip of the solder tip.
- Always choose a solder tip which matches the size of the solder pad as good as possible.

Solder procedure:

- Make sure to use a solder iron which is grounded via the mains supply of the soldering station for ESD protection.
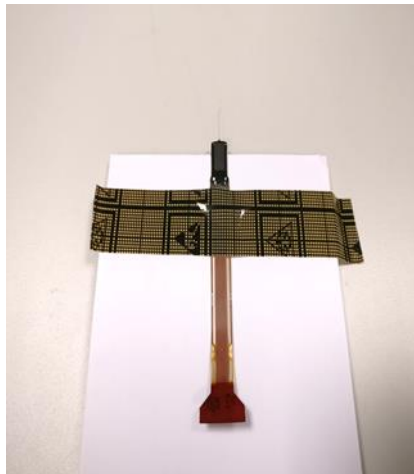- Fix the probe to a clean surface. A good method is to use ESD tape. (Figure 41)



*Figure 41: Fixing the probe before soldering.*

- Clean the solder tip using a brass wire mesh or damp sponge. Repeat at frequent intervals.
- Wet the solder tip slightly with solder wire. This improves heat transfer from the iron to the solder pad.
- Insert the wire through the hole in the solder pad. Place the solder iron at the corner between the pad and the GND/REF wire. (Figure 42)
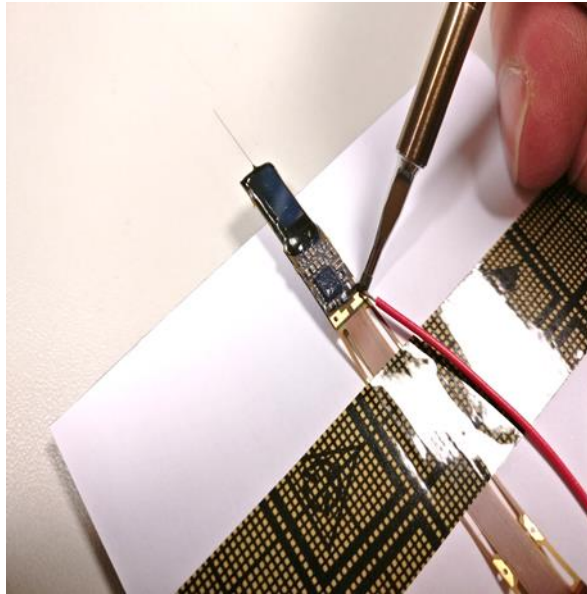
*Figure 42: Placing the solder tip in the corner between wire and pad.*

- Feed a small amount of solder to the corner between the solder tip and wire. The solder melts on the pad and the GND/REF wire. Solder wire can be purchased in different diameters. For this application it is advisable to use a smaller diameter (< 1 mm), also depending on the diameter of the GND/REF wire.
- The soldering time and temperature should be minimized to <4 s and max. 350°C, respectively.
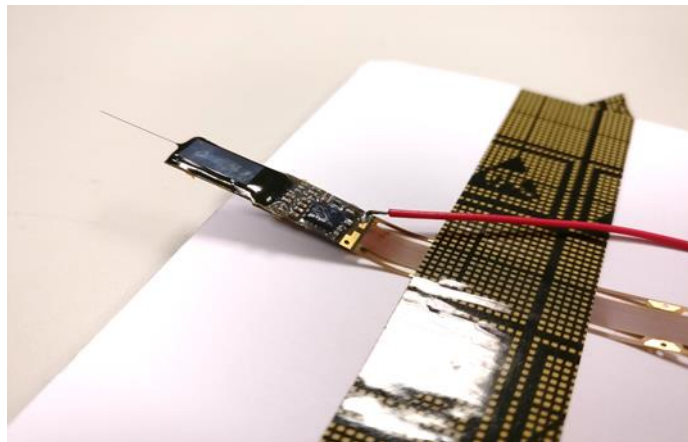


*Figure 43: Wire soldered to the solder pad.*

An alternative method does not make use of the hole in the solder pad:
- Apply some solder to the solder pad and GND/REF wire separately. (Figure 44)
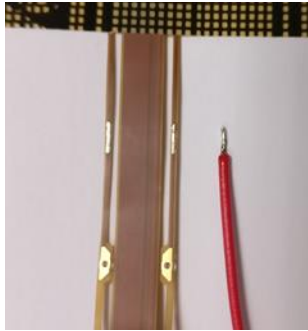
*Figure 44: Solder applied to solder pad and GND/REF wire separately.*

- Place the GND/REF wire on top of the solder pad.
- Press the solder tip on top of the GND/REF wire and feed some amount of solder wire. This forms a strong solder joint. (Figure 45)
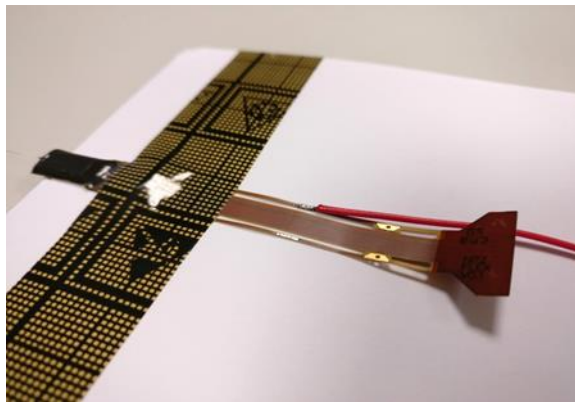


*Figure 45: Soldered wire to solder pad without hole.*

Always inspect the quality of the solder joint under a microscope before implanting. Also check the components surrounding the solder pads for eventual damage. Run the built-in self-tests after soldering to check the functionality of the probe.

IMPORTANT: Generally, poor connections are a common source of noise. The reference and ground connections on the probe and flex are critical as they are very close to the probe signal amplifiers.

# Appendix C    ESD Safety

To avoid ESD damage when handling the electronic hardware (probe, HS, PXIe), the operator must be grounded via ESD protective equipment, such as a wrist wrap. General ESD guidelines can be found at: http://www.esda.org/about-esd/esd-fundamentals/part-3-basic-esd-control-procedures-and-materials/.

When the probe is implanted in an animal, special precautions are required; In order to protect the probe from ESD damage, potential static charge build-up on the animal must be discharged via a low-current path. ESD-compliant material must be used, because the cables and connectors have an integrated 1M-10M resistor, which limits the current and thus induces a slow discharge rather than a spike.

Preventing static charge build-up on an animal can be challenging, especially when the animal is transported between locations (e.g., vivarium cage, transport cage, lab cage, operation table). Static charge build-up can be prevented by continuously keeping the animal on an ESD-compliant mat which is connected to earth ground via an ESD-compliant cable.

If continuous grounding of the animal is not feasible, the following guidelines should be followed:
- Grounding of the operator via ESD-compliant protective equipment when touching the animal.
- Grounding of the animal via ESD-compliant protective equipment prior to connecting the probe flex to the HS. This can be done, for example, by placing the animal on an ESD-compliant mat. Alternatively, if the external reference wire of the probe flex is connected to the animal's skull, the grounding can be done through this connection. This connection should be maintained throughout the experiment.
- Grounding of the probe flex ground pin or wire via ESD-compliant protective equipment prior to connecting the probe flex to the HS. This connection can be removed when the probe flex is plugged into the HS.
- Grounding of the PXIe module to earth ground prior to connecting the probe flex to the HS. This is normally already achieved if the PXIe chassis is plugged into the mains supply.

**NOTE**: *A connection from the probe to the PXIe acquisition module ground does not provide an ESD-safe discharge path, because it does not contain a current-limiting resistor.*